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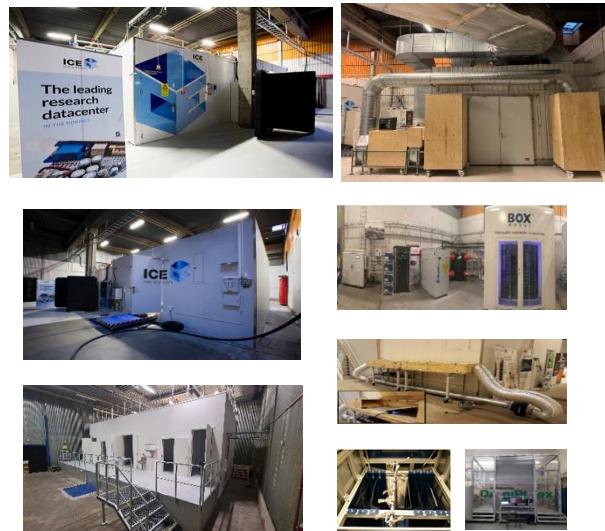
# Exploring the HIGHER Standard: Validating European Silicon for the Digital Decade

RISE – Research Institutes of Sweden

# RISE



A full-scale research data centre and test environment with the objective to increase knowledge, strengthen the AI & data centre ecosystems and attract researchers.



- 30+ projects, from the ground to the cloud
- 25 employees
- 4 M EUR annual turnover
- Established 2016

Partners: Ericsson, ABB, Vattenfall, Meta, LTU, Region North, Vertiv, BP Castrol...



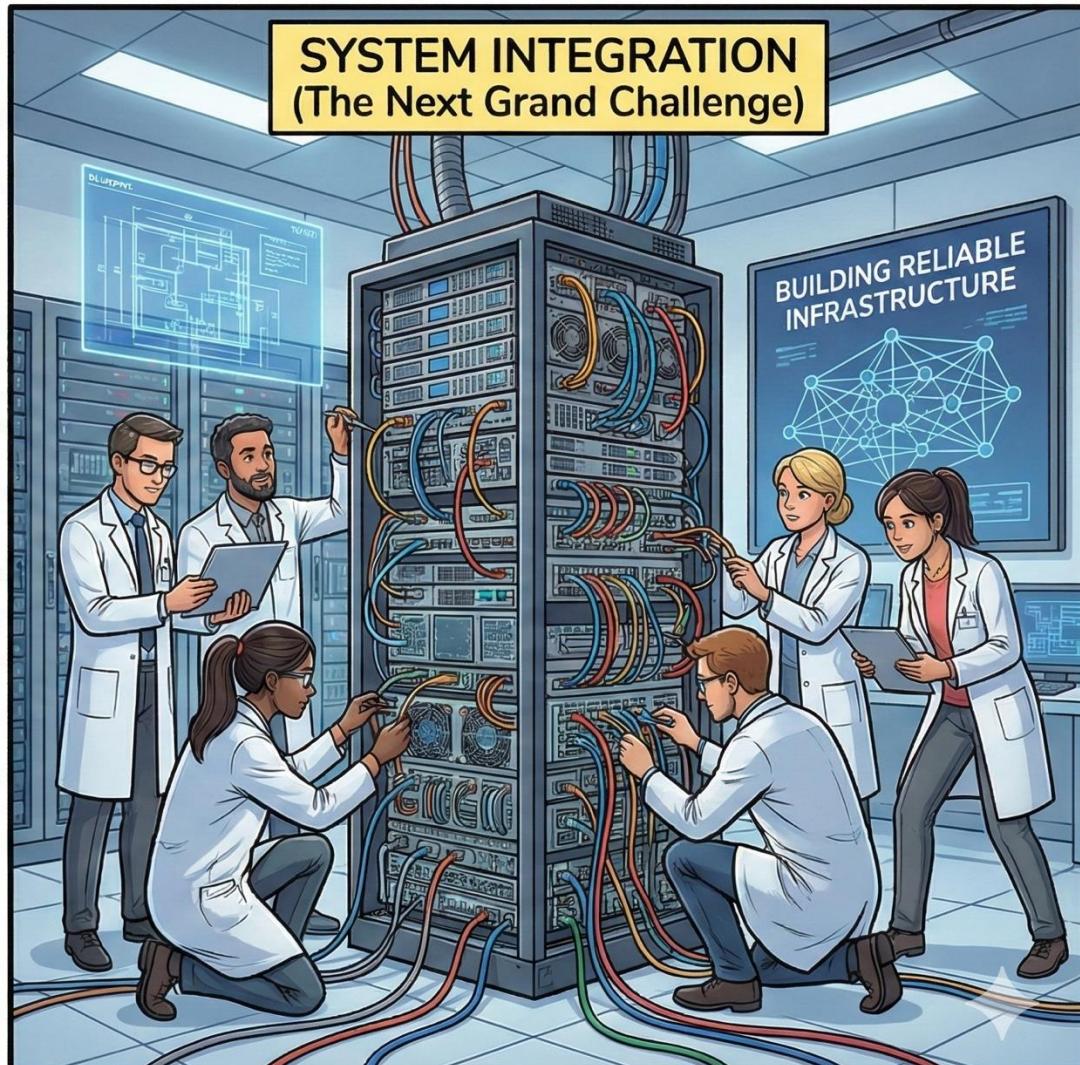
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# From Silicon Success to System Synergy: The European Digital Decade

## EUROPEAN CHIPS (A Vision Realized)

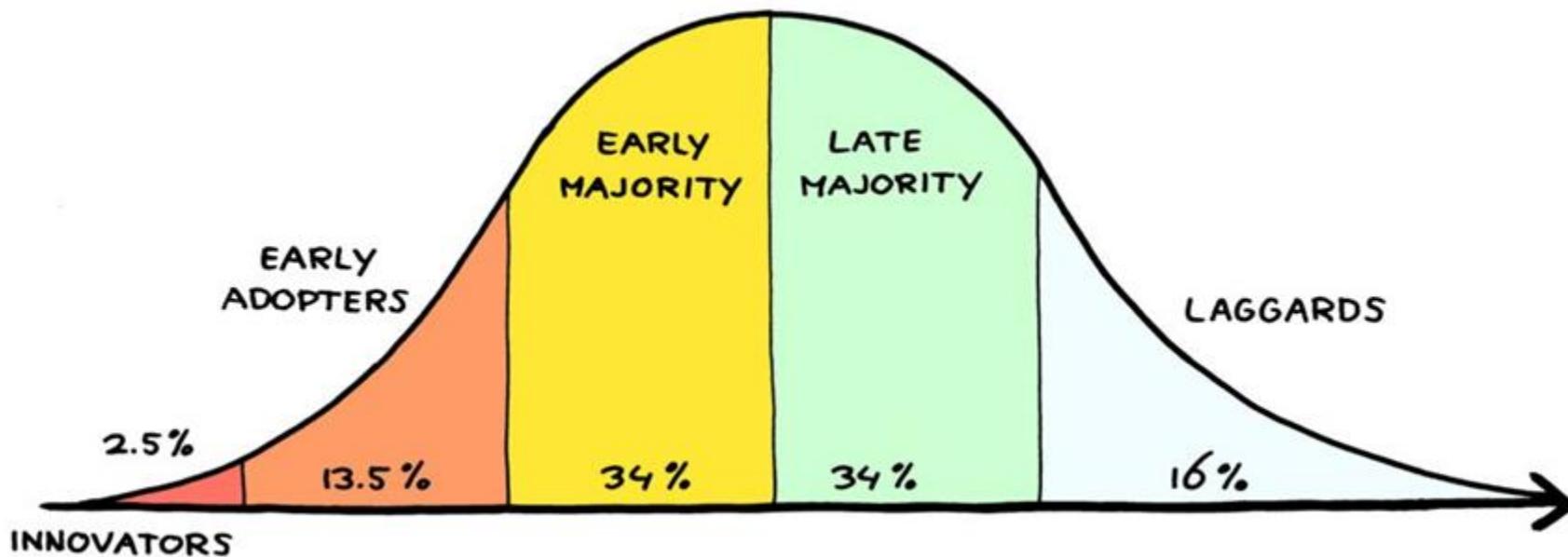


## SYSTEM INTEGRATION (The Next Grand Challenge)



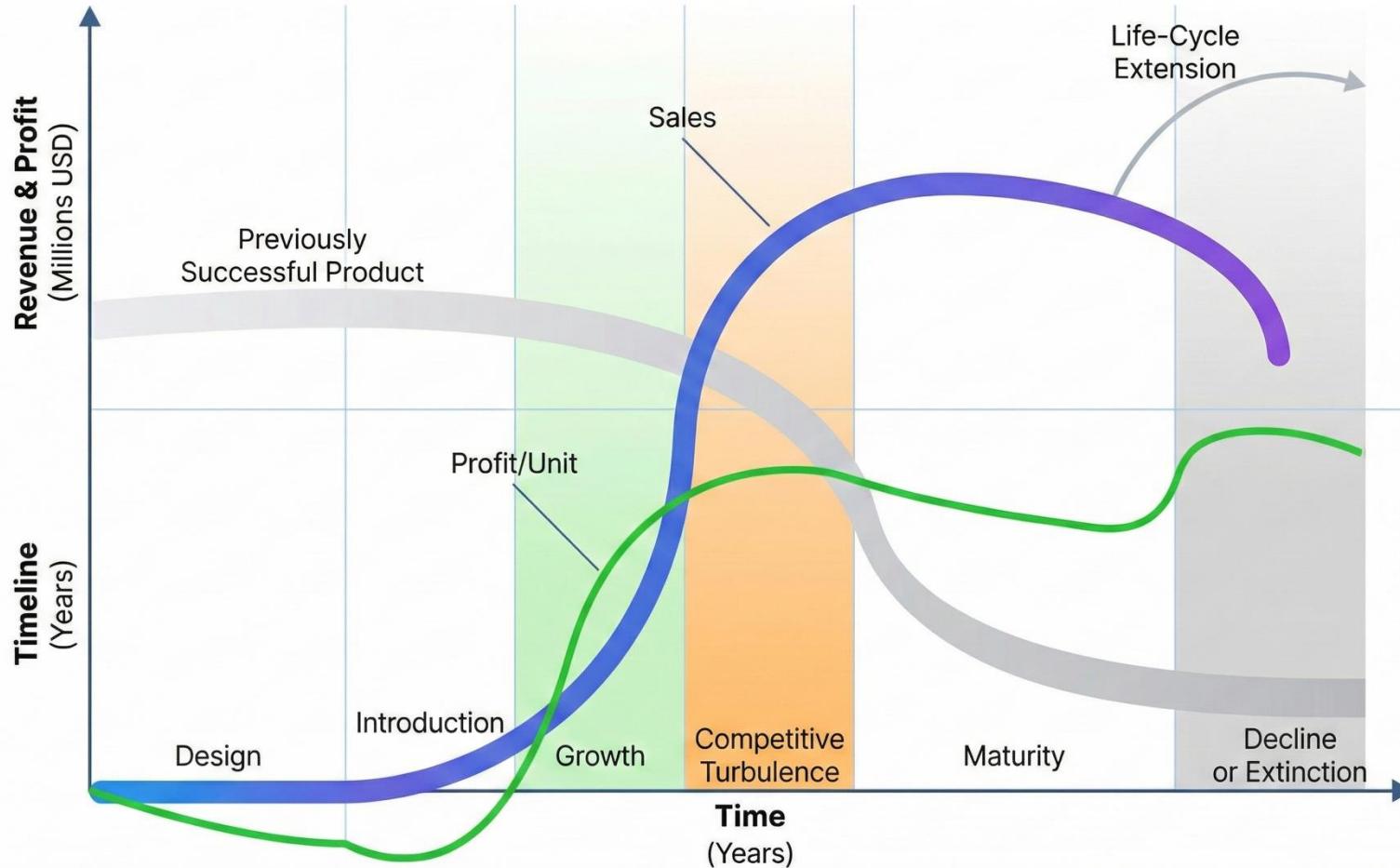
# Technology validation

Technology validation is the process of proving a new technology works as intended and meets real-world needs, often through prototypes and testing in simulated or actual environments, to confirm its feasibility, performance, and value before full-scale development, ensuring it solves real problems, aligns with goals, and minimizes risk.



# The beginning

## Product Life Cycle Stages



# What can go wrong?

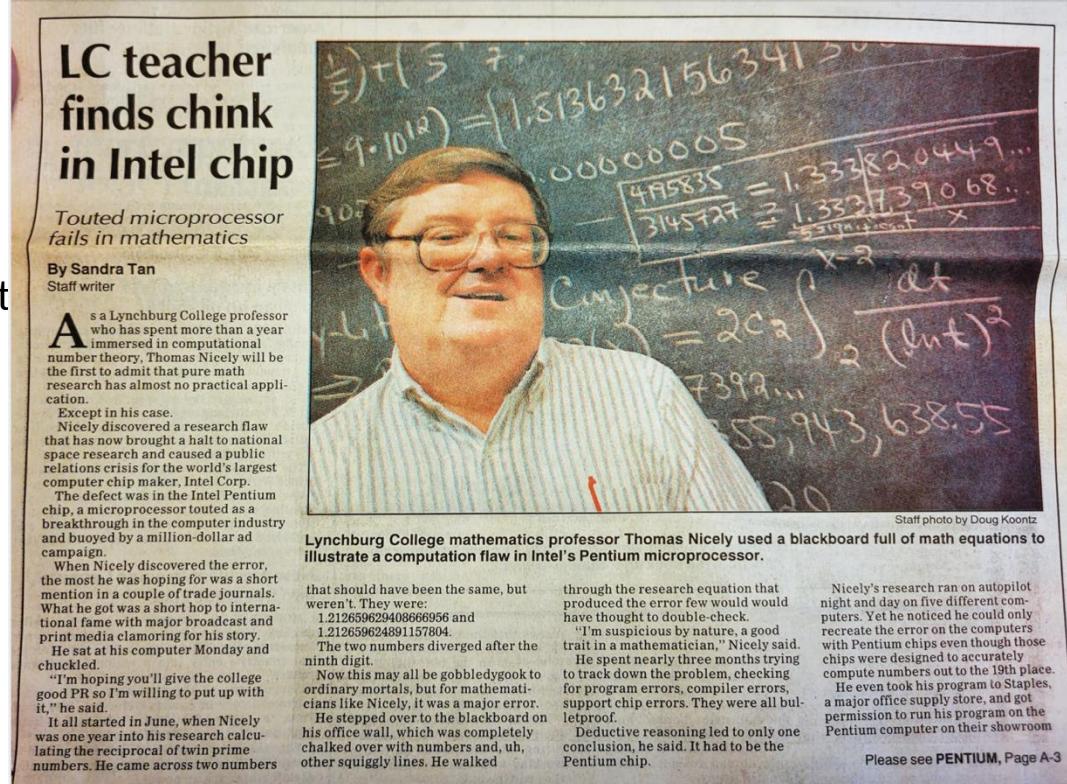
$$\frac{4,195,835}{3,145,727} = 1.333820449136241002$$

$$\frac{4,195,835}{3,145,727} = 1.333739068902037589$$

## Intel Pentium FDIV Bug (1994)

- What happened: A flaw in the floating-point unit of early Pentium processors caused incorrect division results.
- The Cost estimation: The bug estimated to cost Intel ~\$ 475 million (unadjusted for inflation) to replace the chips.

Reference: [https://en.wikipedia.org/wiki/Pentium\\_FDIV\\_bug](https://en.wikipedia.org/wiki/Pentium_FDIV_bug)  
<https://www.facebook.com/groups/LivingInLynchburg/posts/3464126760513113/>



**LC teacher finds chink in Intel chip**

*Touted microprocessor fails in mathematics*

By Sandra Tan  
Staff writer

**A**s a Lynchburg College professor who has spent more than a year immersed in computational number theory, Thomas Nicely will be the first to admit that pure math research has almost no practical application. Except in his case.

Nicely discovered a research flaw that has now brought a halt to national space research and caused a public relations crisis for the world's largest computer chip maker, Intel Corp.

The defect was in the Intel Pentium chip, a microprocessor touted as a breakthrough in the computer industry and buoyed by a million-dollar ad campaign.

When Nicely discovered the error, the most he was hoping for was a short mention in a couple of trade journals. What he got was a short hop to international fame with major broadcast and print media clamoring for his story.

He sat at his computer Monday and chuckled.

"I'm hoping you'll give the college good PR so I'm willing to put up with it," he said.

It all started in June, when Nicely was one year into his research calculating the reciprocal of twin prime numbers. He came across two numbers

that should have been the same, but weren't. They were: 1.212659629408666956 and 1.212659624891157804.

The two numbers diverged after the ninth digit.

Now this may all be gobbledegook to ordinary mortals, but for mathematicians like Nicely, it was a major error.

He stepped over to the blackboard on his office wall, which was completely chalked over with numbers and, uh, other squiggly lines. He walked

through the research equation that produced the error few would have thought to double-check.

"I'm suspicious by nature, a good trait in a mathematician," Nicely said. He spent nearly three months trying to track down the problem, checking for program errors, compiler errors, support chip errors. They were all bulletproof.

Deductive reasoning led to only one conclusion, he said. It had to be the Pentium chip.

Staff photo by Doug Koontz

Lynchburg College mathematics professor Thomas Nicely used a blackboard full of math equations to illustrate a computation flaw in Intel's Pentium microprocessor.

Nicely's research ran on autopilot night and day on five different computers. Yet he noticed he could only recreate the error on the computers with Pentium chips even though those chips were designed to accurately compute numbers out to the 19th place. He even took his program to Staples, a major office supply store, and got permission to run his program on the Pentium computer on their showroom floor.

Please see PENTIUM, Page A-3

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# What can go wrong?

Samsung's investigation into the Galaxy Note7 incidents concluded that the batteries were the cause of the fires. The company identified two separate battery faults from different suppliers that led to the same outcome: overheating and combustion.

Samsung accepted responsibility for failing to identify these design and manufacturing issues during their validation processes. As a result of the investigation, Samsung implemented new safety measures, including an "8-Point Battery Safety Check," to prevent similar incidents in the future. The recall and discontinuation cost Samsung an estimated \$5.3 billion.

Reference: <https://news.samsung.com/global/infographic-galaxy-note7-what-we-discovered>  
<https://www.theguardian.com/technology/2016/oct/10/samsung-halts-production-galaxy-note-7-phone-battery-fires>



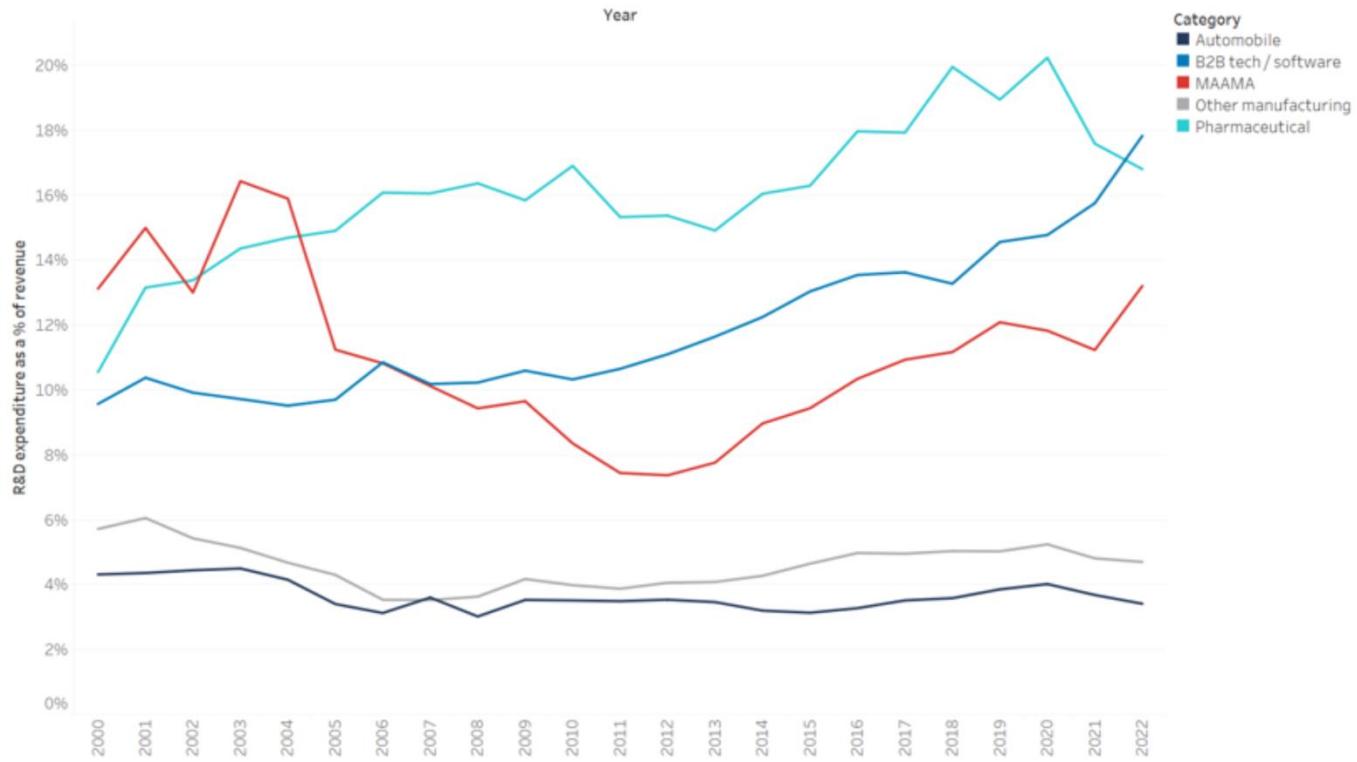
## Galaxy Note7 What we discovered

*A short circuit within the battery may occur when there is damage to the separator that allows the positive and negative electrodes to meet within the jellyroll. Based on a detailed analysis of the affected batteries, both Battery A from the 1st recall and Battery B from the 2nd recall, we identified separate factors that originated in and were specific to the two different batteries.*

### Lithium-Ion Battery Structure

Negative Tab  
Positive Tab  
Separator  
"Jelly Roll"

# Microsoft, Alphabet, Amazon, Meta, and Apple



Reference: Padilla, J., Ginsburg, D. H., & Wong-Ervin, K. W. (2024). DYNAMIC COMPETITION AND ANTITRUST: QUICK-LOOK INFERENCES FROM THE ANALYSIS OF BIG TECH'S R&D EXPENDITURE RATIOS. Forthcoming in the Antitrust Law Journal.

# Technology Readiness Levels

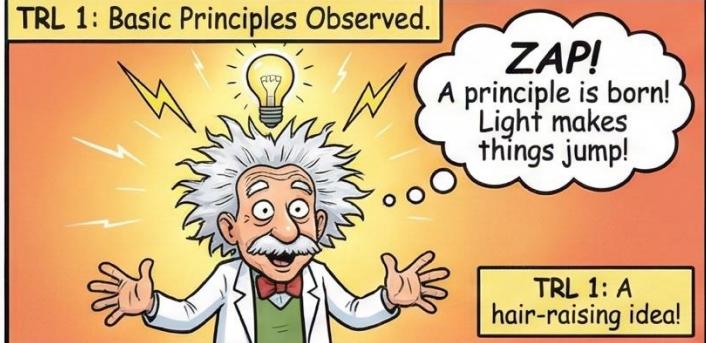
## G. Technology readiness levels (TRL)

Where a topic description refers to a TRL, the following definitions apply, unless otherwise specified:

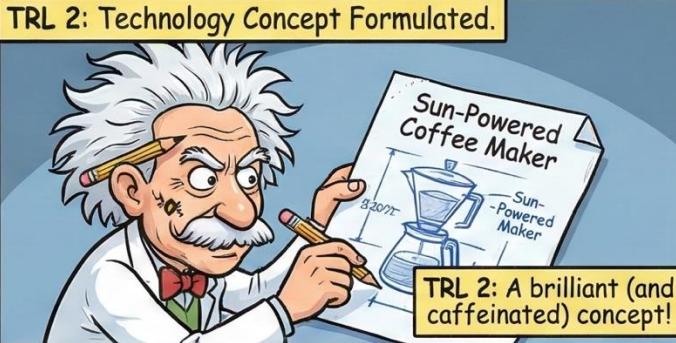
- TRL 1 – basic principles observed
- TRL 2 – technology concept formulated
- TRL 3 – experimental proof of concept
- TRL 4 – technology validated in lab
- TRL 5 – technology validated in relevant environment (industrially relevant environment in the case of key enabling technologies)
- TRL 6 – technology demonstrated in relevant environment (industrially relevant environment in the case of key enabling technologies)
- TRL 7 – system prototype demonstration in operational environment
- TRL 8 – system complete and qualified
- TRL 9 – actual system proven in operational environment (competitive manufacturing in the case of key enabling technologies; or in space)

# The European TRLs: From Spark to Market-Ready Mayhem!

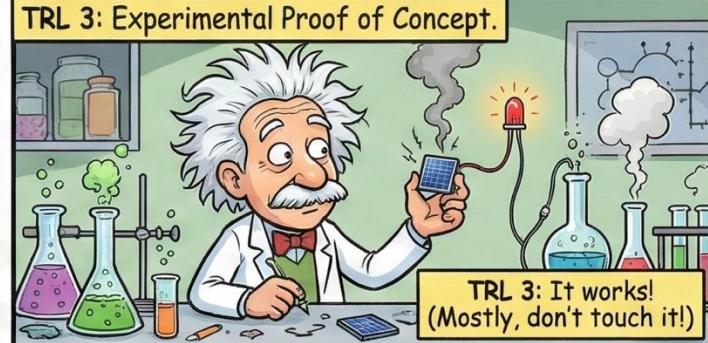
TRL 1: Basic Principles Observed.



TRL 2: Technology Concept Formulated.



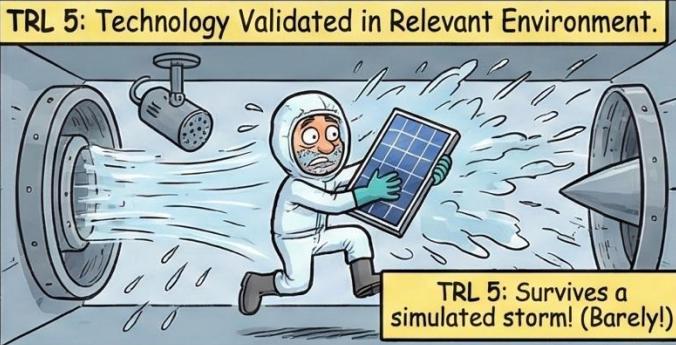
TRL 3: Experimental Proof of Concept.



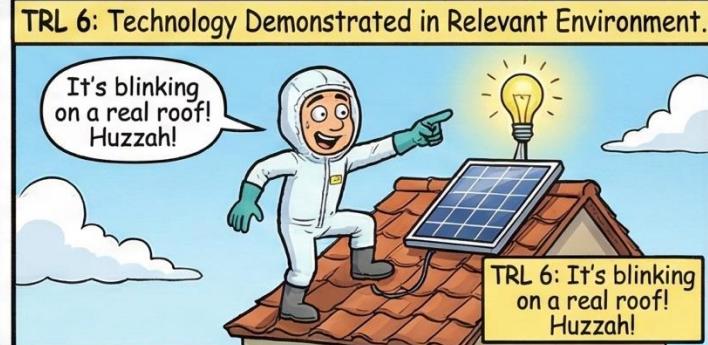
TRL 4: Technology Validated in Lab.



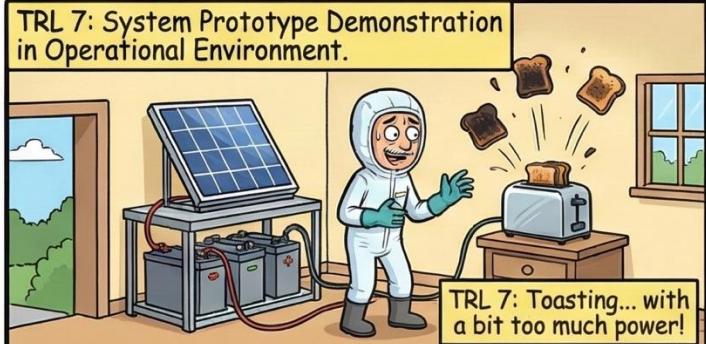
TRL 5: Technology Validated in Relevant Environment.



TRL 6: Technology Demonstrated in Relevant Environment.



TRL 7: System Prototype Demonstration in Operational Environment.



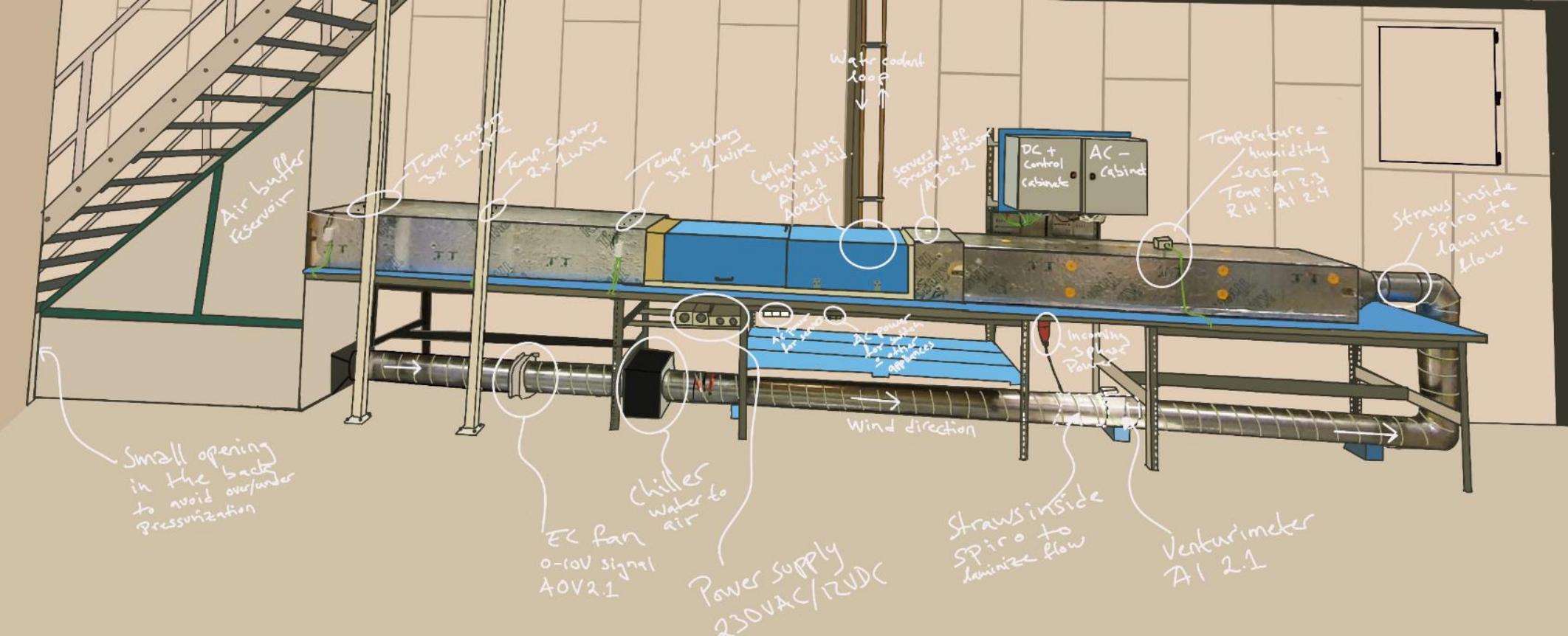
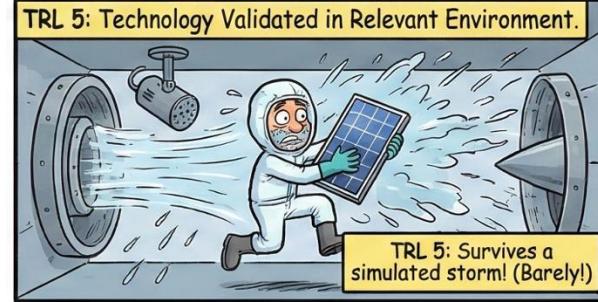
TRL 8: System Complete and Qualified.



TRL 9: Actual System Proven in Operational Environment.

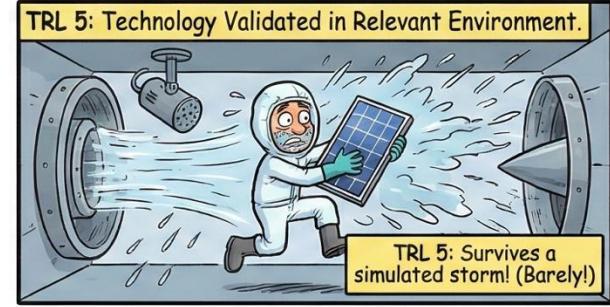
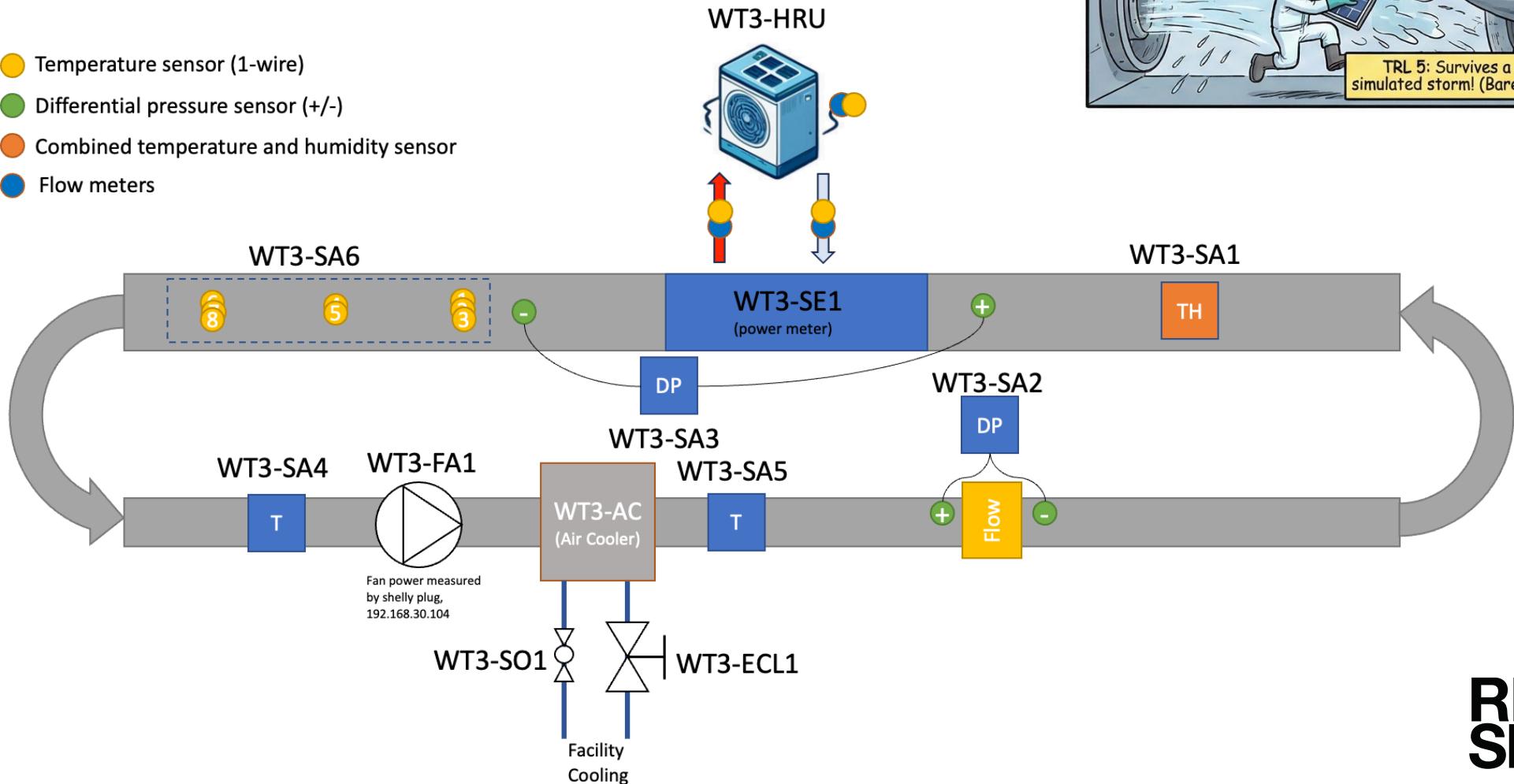


# Rerevant environment



# Rerevant environment

- Temperature sensor (1-wire)
- Differential pressure sensor (+/-)
- Combined temperature and humidity sensor
- Flow meters

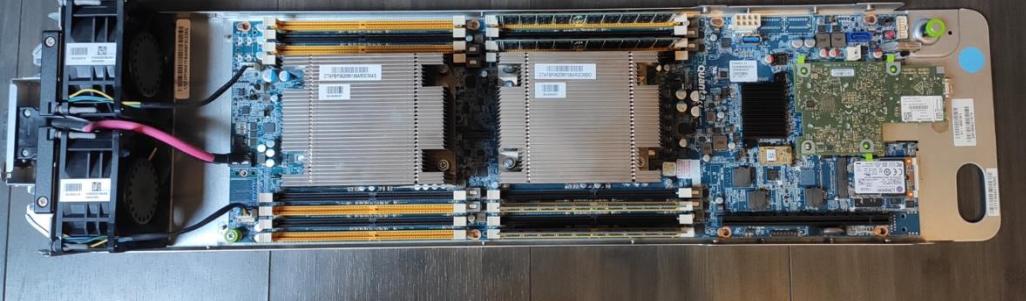
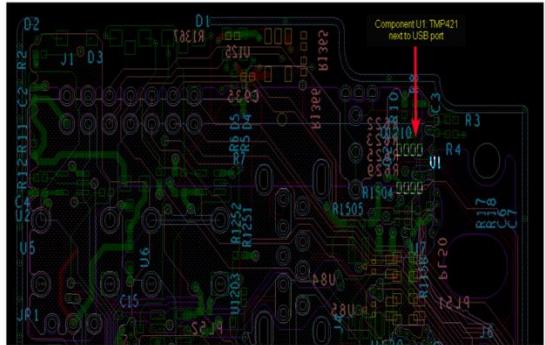


# Paying attention to the data



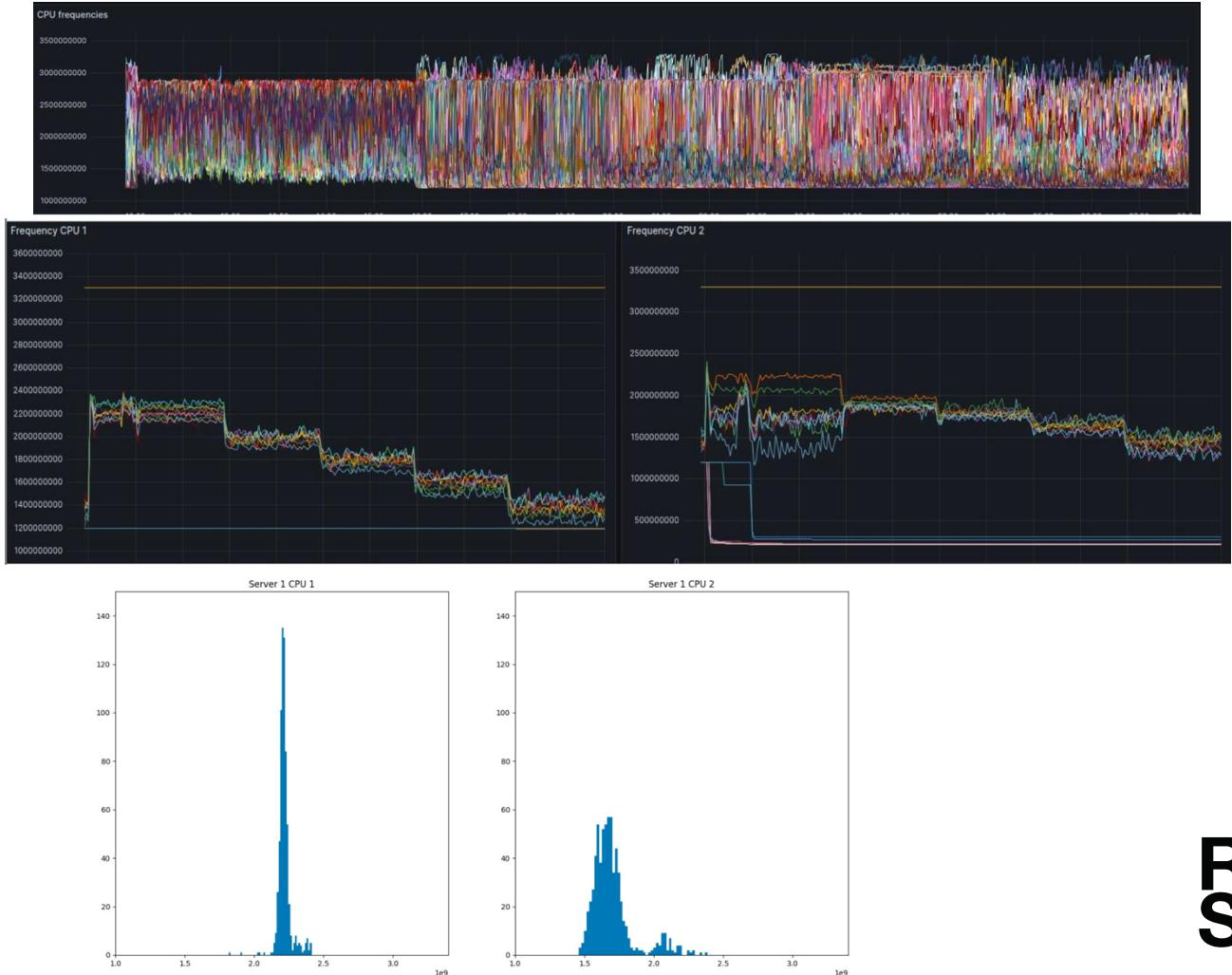
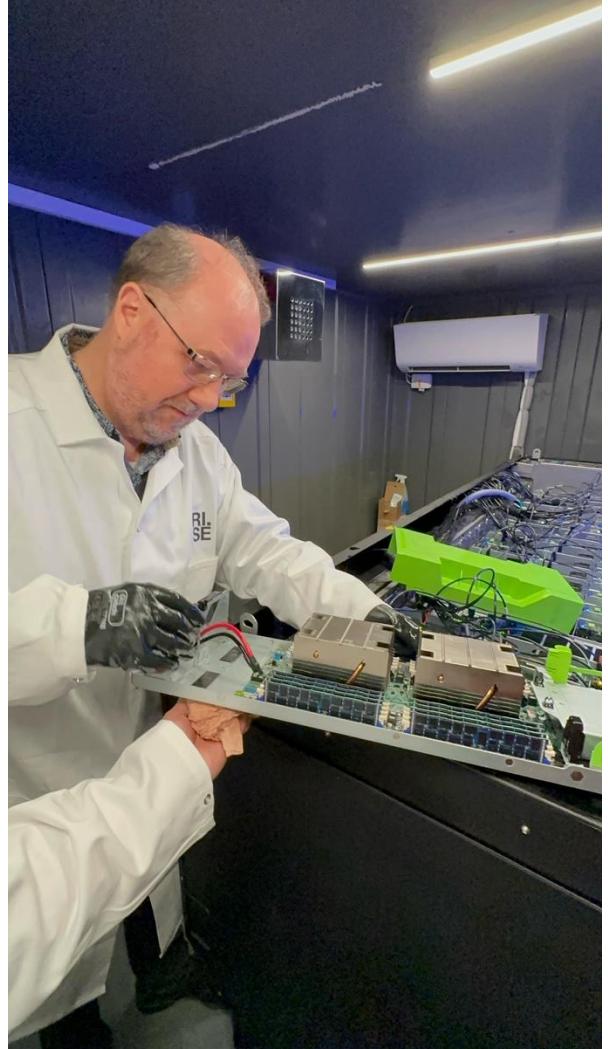
```
ipmitool s lanplus -U UEBD -P PASSWORD -d 192.168.0.107 sensor
P0 Temp | 24.000 | degrees C | ok | na | na | na | na | 91.000 | na
P1 Temp | 24.000 | degrees C | ok | na | na | na | na | 104.000 | na
P0 DTSmx | 95.000 | degrees C | ok | na | na | na | na | na | na
P1 DTSmx | na | degrees C | na | na | na | na | na | na | na
P0 Therm Margin | -71.000 | degrees C | ok | na | na | na | na | -4.000 | na
P1 Therm Margin | -71.000 | degrees C | ok | na | na | na | na | -4.000 | na
P3V3 | 3.307 | Volts | ok | na | 1.297 | na | na | 3.625 | na
P5V | 5.009 | Volts | ok | na | 4.501 | na | na | 5.493 | na
P12V | 12.120 | Volts | ok | na | 11.350 | na | na | 13.200 | na
P0 VOTS_STB | 1.959 | Volts | ok | na | 1.951 | na | na | 1.947 | na
P1V8_AUX | 1.793 | Volts | ok | na | 1.627 | na | na | 1.980 | na
P3V3_AUX | 3.323 | Volts | ok | na | 2.973 | na | na | 3.625 | na
P5V_AUX | 5.009 | Volts | ok | na | 4.501 | na | na | 5.493 | na
P12V_AUX | 3.307 | Volts | ok | na | 2.726 | na | na | 3.625 | na
Inlet Temp | 25.000 | degrees C | ok | na | na | na | na | 40.000 | na
Outlet Temp | 25.000 | degrees C | ok | na | na | na | na | 40.000 | na
PCH Temp | 31.000 | degrees C | ok | na | na | na | na | 65.000 | na
HSC Input Volt | 12.000 | Volts | ok | na | 11.300 | na | na | 13.200 | na
HSC Input Power | 51.000 | Watts | ok | na | na | na | na | 501.000 | na
HSC Temp | 16.000 | degrees C | ok | na | na | na | na | 86.000 | na
HSC Sls Low | 0x0 | discrete | 0x0000 | na | na | na | na | na | na
HSC Sls High | 0x0 | discrete | 0x0000 | na | na | na | na | na | na
HSC Core Curr | 4.200 | Amps | ok | na | 1.478 | na | na | 9.000 | na
SYS FAN0 | 2000.000 | RPMs | ok | na | 500.000 | na | na | 9000.000 | na
SYS FAN1 | 2000.000 | RPMs | ok | na | 500.000 | na | na | 9000.000 | na
P0 VR Temp | 24.000 | degrees C | ok | na | na | na | na | 92.000 | na
P0 VR Volt | 1.220 | Volts | ok | na | 1.150 | na | na | 1.250 | na
P0 VR Curr | 8.500 | Amps | ok | na | na | na | na | 108.000 | na
P0 core VR Curr | 8.500 | Amps | ok | na | na | na | na | 108.000 | na
P0 core VR POUT | 19.000 | Watts | ok | na | na | na | na | 240.000 | na
P0 core VR PIN | 19.000 | Watts | ok | na | na | na | na | 240.000 | na
P1 VR Temp | 25.000 | degrees C | ok | na | na | na | na | 92.000 | na
P1 core VR Volt | 1.220 | Volts | ok | na | 1.150 | na | na | 1.250 | na
P1 core VR Curr | 8.500 | Amps | ok | na | na | na | na | 108.000 | na
P1 core VR Curr | 8.500 | Amps | ok | na | na | na | na | 108.000 | na
P1 core VR POUT | 19.000 | Watts | ok | na | na | na | na | 240.000 | na
P1 core VR PIN | 19.000 | Watts | ok | na | na | na | na | 240.000 | na
P0 DIMM VR0 Vol | 1.220 | Volts | ok | na | 1.150 | na | na | 1.250 | na
P0 DIMM VR0 Curr | 6.000 | Amps | ok | na | na | na | na | 69.000 | na
P0 DIMM VR0 Temp | 24.000 | degrees C | ok | na | na | na | na | 83.000 | na
P0 DIMM VR0 PIN | 6.000 | Watts | ok | na | 1.150 | na | na | 1.250 | na
P0 DIMM VR0 POUT | 6.000 | Watts | ok | na | na | na | na | 69.000 | na
P0 DIMM VR1 Vol | 1.220 | Volts | ok | na | 1.150 | na | na | 1.250 | na
P0 DIMM VR1 Curr | 6.000 | Amps | ok | na | na | na | na | 69.000 | na
P0 DIMM VR1 Temp | 24.000 | degrees C | ok | na | na | na | na | 83.000 | na
P0 DIMM VR1 PIN | 6.000 | Watts | ok | na | 1.150 | na | na | 1.250 | na
P0 DIMM VR1 POUT | 6.000 | Watts | ok | na | na | na | na | 69.000 | na
P1 DIMM VR0 Vol | 1.220 | Volts | ok | na | 1.150 | na | na | 1.250 | na
P1 DIMM VR0 Curr | 6.000 | Amps | ok | na | na | na | na | 69.000 | na
P1 DIMM VR0 Temp | 24.000 | degrees C | ok | na | na | na | na | 83.000 | na
P1 DIMM VR0 PIN | 6.000 | Watts | ok | na | 1.150 | na | na | 1.250 | na
P1 DIMM VR0 POUT | 6.000 | Watts | ok | na | na | na | na | 69.000 | na
P1 DIMM VR1 Vol | 1.220 | Volts | ok | na | 1.150 | na | na | 1.250 | na
P1 DIMM VR1 Curr | 6.000 | Amps | ok | na | na | na | na | 69.000 | na
P1 DIMM VR1 Temp | 24.000 | degrees C | ok | na | na | na | na | 83.000 | na
P1 DIMM VR1 PIN | 6.000 | Watts | ok | na | 1.150 | na | na | 1.250 | na
P1 DIMM VR1 POUT | 6.000 | Watts | ok | na | na | na | na | 69.000 | na
P1 Package Power | 0.000 | Watts | ok | na | na | na | na | na | na
P0 DIMM0 Temp | 20.000 | degrees C | ok | na | na | na | na | 81.000 | na
P0 DIMM1 Temp | 22.000 | degrees C | ok | na | na | na | na | 81.000 | na
P0 DIMM2 Temp | 22.000 | degrees C | ok | na | na | na | na | 81.000 | na
P0 DIMM3 Temp | 22.000 | degrees C | ok | na | na | na | na | 81.000 | na
C1 Local Temp | 0.000 | degrees C | ok | na | na | na | na | 94.000 | na
C1 Remote Temp | 82.000 | degrees C | ok | na | na | na | na | 95.000 | na
C2 Local Temp | 0.000 | degrees C | ok | na | na | na | na | 94.000 | na
C2 Remote Temp | 1.000 | degrees C | na | na | na | na | na | 93.000 | na
C3 Local Temp | 0.000 | degrees C | na | na | na | na | na | 94.000 | na
C3 Remote Temp | 0.000 | degrees C | na | na | na | na | na | 83.000 | na
C4 Local Temp | 0.000 | degrees C | na | na | na | na | na | 94.000 | na
C4 Remote Temp | 0.000 | degrees C | na | na | na | na | na | 93.000 | na
CPU0 Error | 0x0 | discrete | 0x0000 | na | na | na | na | na | na
CPU1 Error | na | discrete | na | na | na | na | na | na | na
P0_CH0DIMM0_Sts | 0x0 | discrete | 0x0080 | na | na | na | na | na | na
P0_CH0DIMM1_Sts | 0x0 | discrete | 0x0080 | na | na | na | na | na | na
P0_CH1DIMM0_Sts | 0x0 | discrete | 0x0080 | na | na | na | na | na | na
P0_CH1DIMM1_Sts | 0x0 | discrete | 0x0080 | na | na | na | na | na | na
P0_CH2DIMM0_Sts | 0x0 | discrete | 0x0080 | na | na | na | na | na | na
P0_CH2DIMM1_Sts | 0x0 | discrete | 0x0080 | na | na | na | na | na | na
P0_CH3DIMM0_Sts | 0x0 | discrete | 0x0080 | na | na | na | na | na | na
P0_CH3DIMM1_Sts | 0x0 | discrete | 0x0080 | na | na | na | na | na | na
SEL Status | 0x0 | discrete | 0x0081 | na | na | na | na | na | na
DCM Powerchdgd | 0x0 | discrete | 0x0000 | na | na | na | na | na | na
NTP Status | 0x0 | discrete | 0x0000 | na | na | na | na | na | na
Chassis Pwr Sts | 0x0 | discrete | 0x0180 | na | na | na | na | na | na
VR HOT | 0x0 | discrete | 0x0080 | na | na | na | na | na | na
VR_DMM_Hot | 0x0 | discrete | 0x0000 | na | na | na | na | na | na
CPU_DMM_Hot | 0x0 | discrete | 0x0000 | na | na | na | na | na | na
Autosave | 1 | tcm | na | na
Sys booting stt | 0x0 | discrete | 0x0080 | na | na | na | na | na | na
System Status | 0x0 | discrete | 0x0180 | na | na | na | na | na | na
```

Inlet Temperature at Component U1 next to USB port on Front (U1 is visible on top on board):

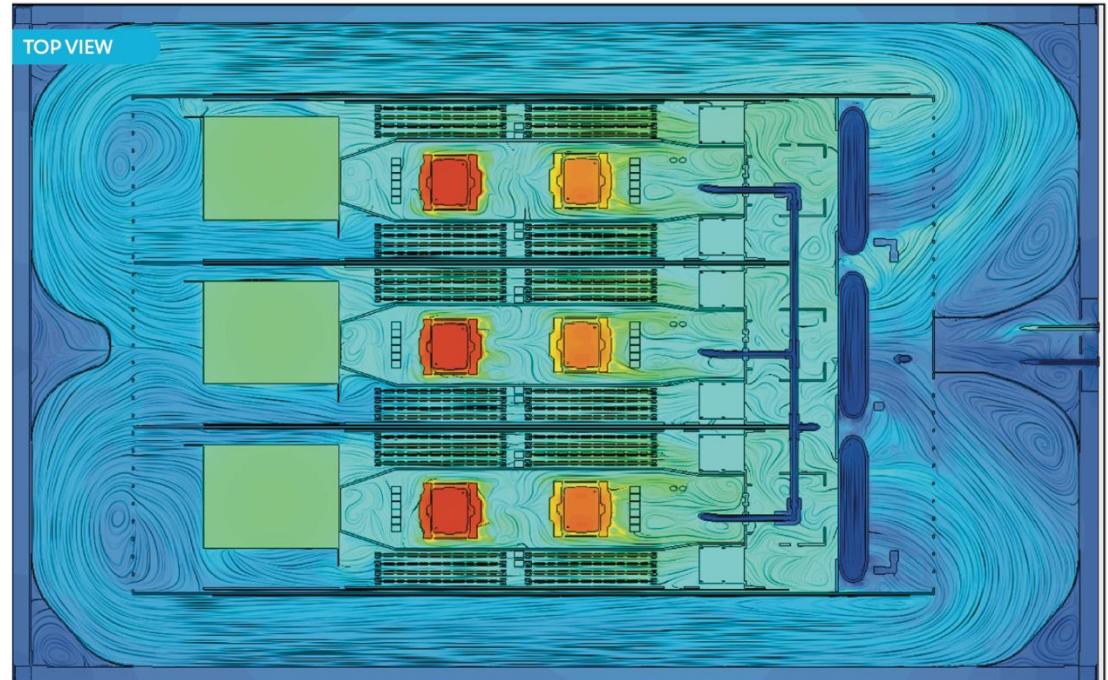
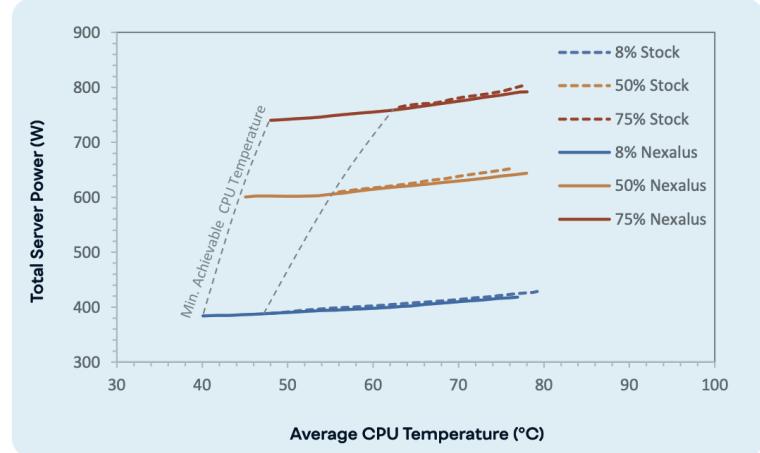
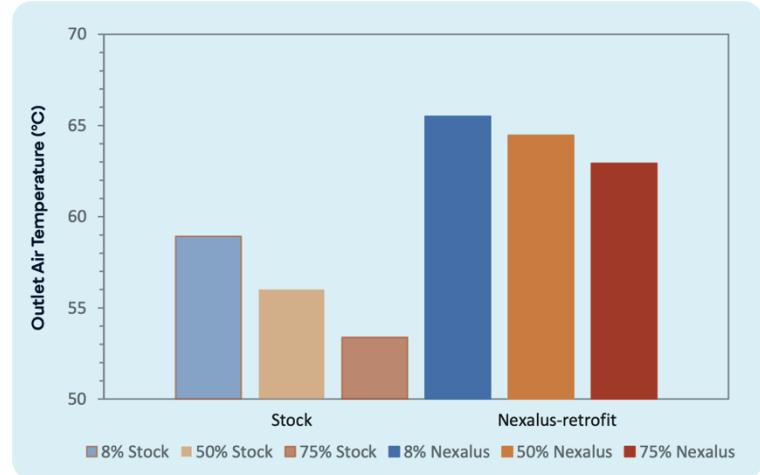


The IPMI sensor command reports a lot of sensor data. Leopard V2 servers' board management system collects data from 144 points. The BMC, which has direct access to all analogue sensors on the motherboard or through the PCH Management Engine, reports this data for sustainable server operation.

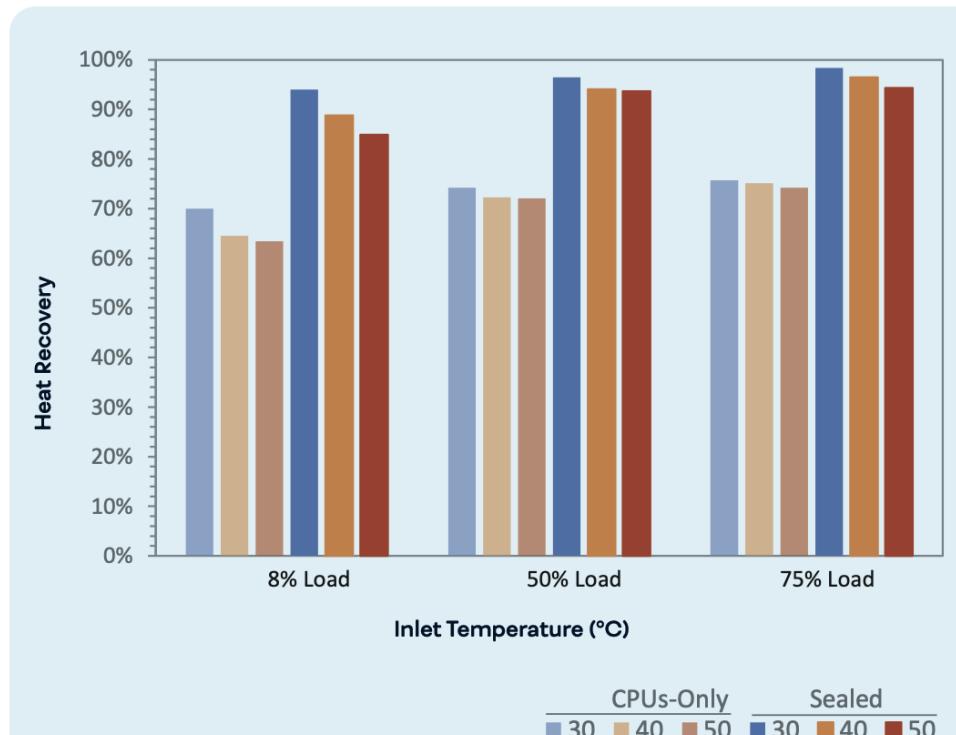
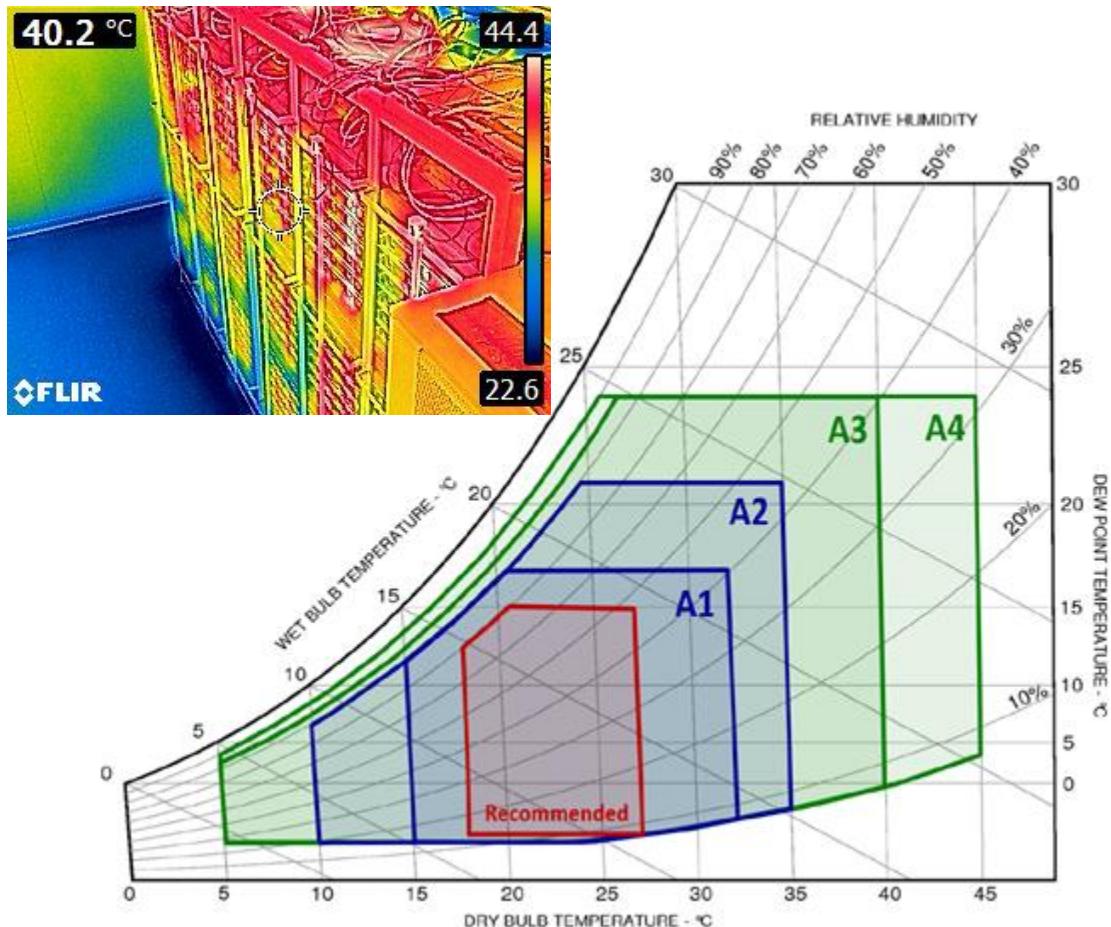
# Importance of data



# Understanding performance



# Complying with the standards

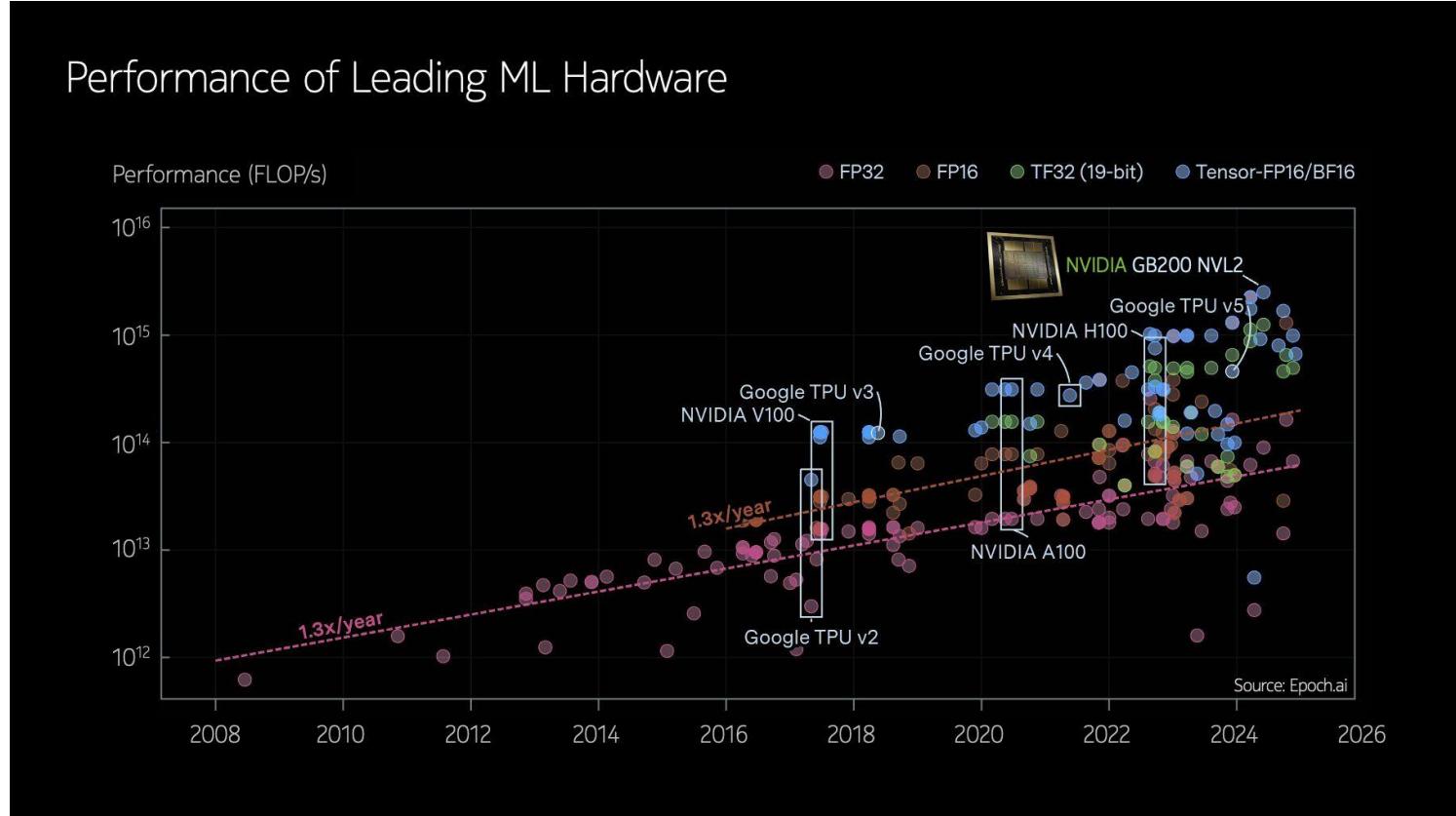


# AI model compute requirements

Computing Demand is Growing: Training



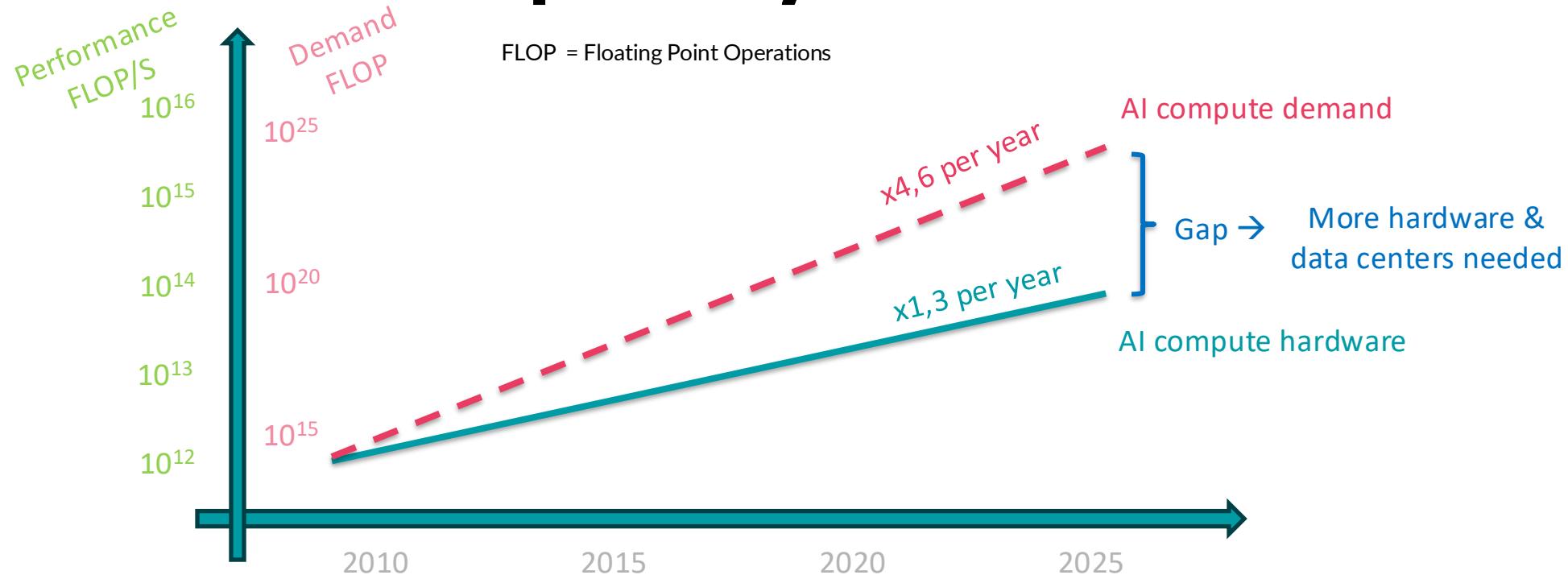
# AI compute hardware capabilities



Demand is  
x4.6 per  
year

Hardware is  
x1.3 per  
year

# AI compute demand & hardware capability

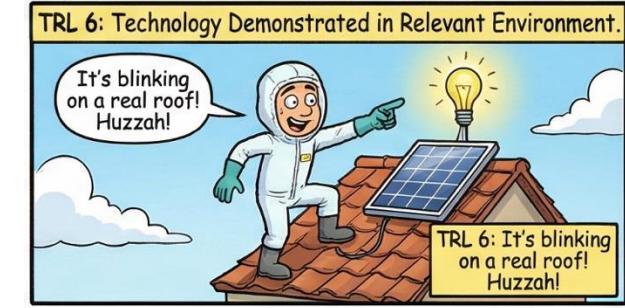
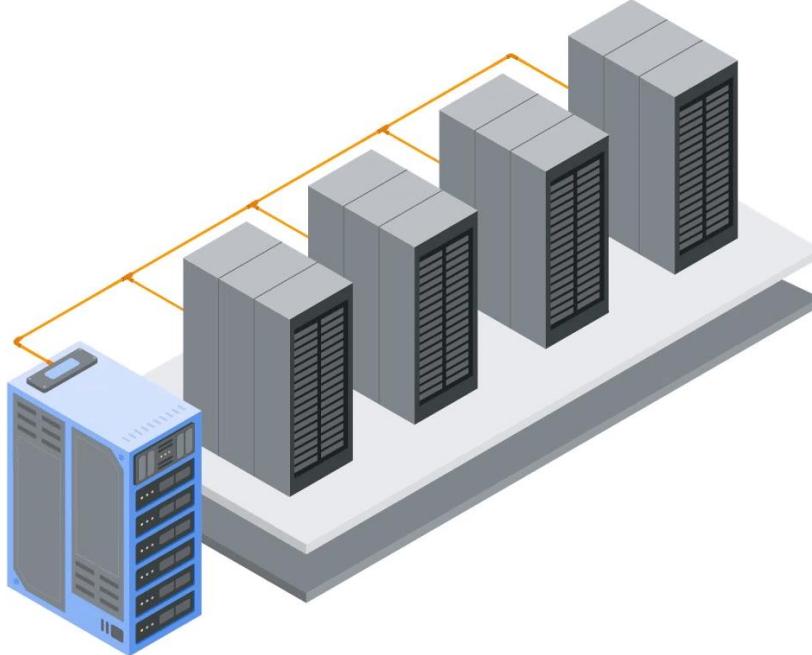


Message: The widening gap between AI compute demand and the pace of hardware performance improvements is a key driver behind rising energy use and the surge in data centre investments.



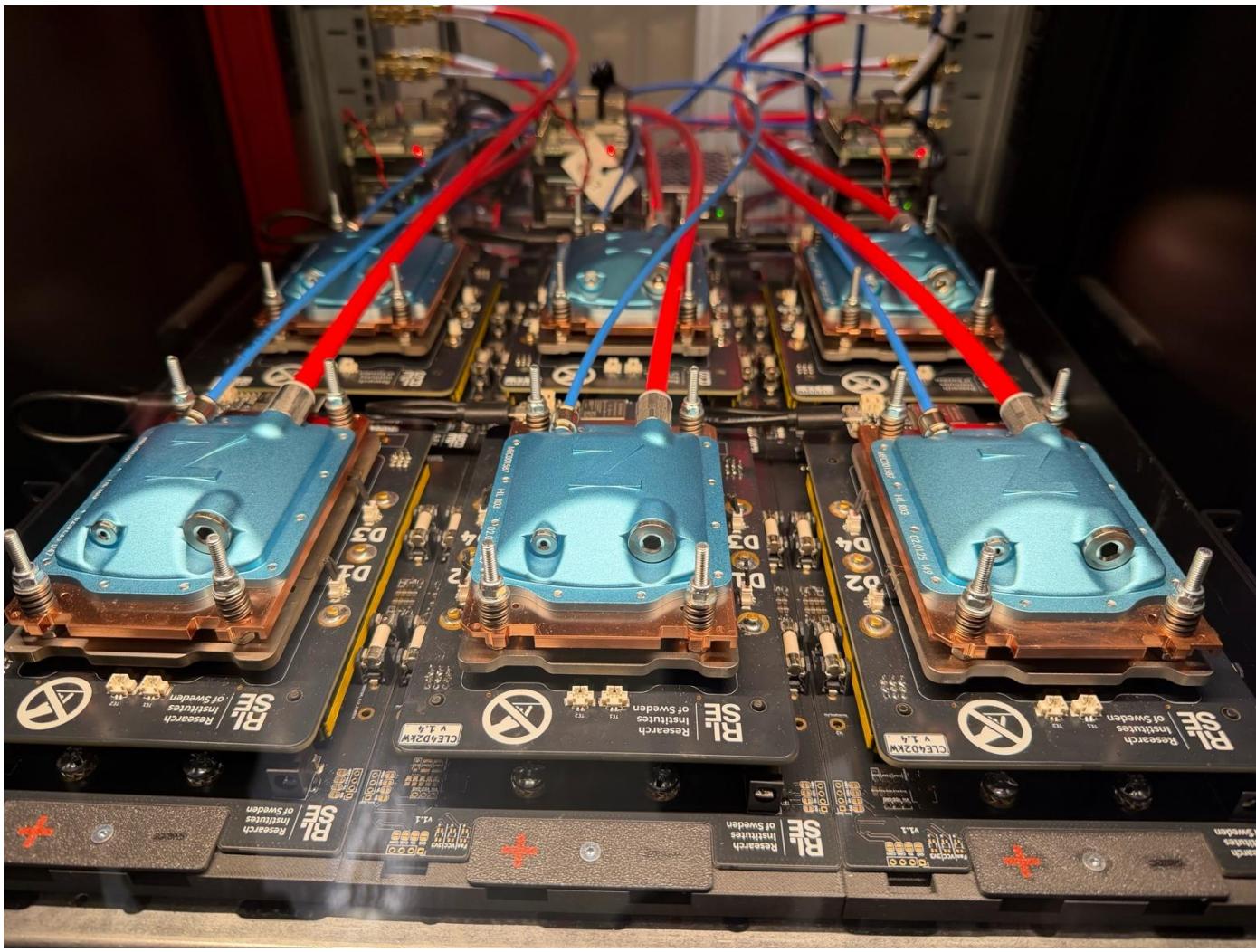
# AI infrastructure is hot. New power distribution and liquid cooling infrastructure can help

## Transforming power delivery with 1 MW per IT rack

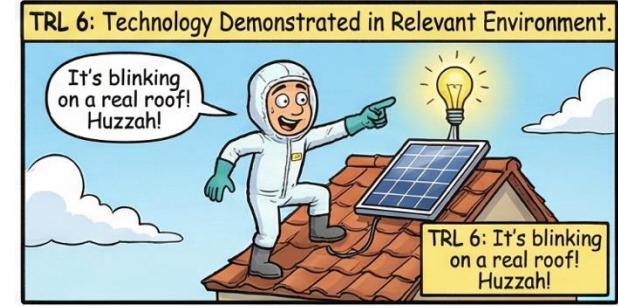


Reference: <https://cloud.google.com/blog/topics/systems/enabling-1-mw-it-racks-and-liquid-cooling-at-ocp-emea-summit>

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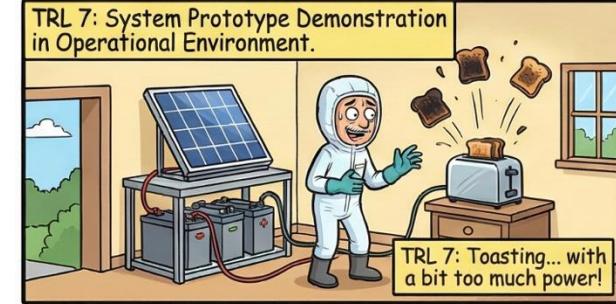
Reference: <https://www.ri.se/en/our-first-2u-server-emulator-of-12-kw-under-test>



Chip load emulators (CLEs):  
CLEs, can reach 2kW each. CLEs are fully load and temperature controlled. They are designed to evaluate cooling performance of coldplates, 1- or 2-phase systems cooling systems, immersion solutions, air cooling or hybrid cooling units at high heatflux. It will then be possible to reach 30 kW in 2U or up to 700 kW in a full sized 19" rack.

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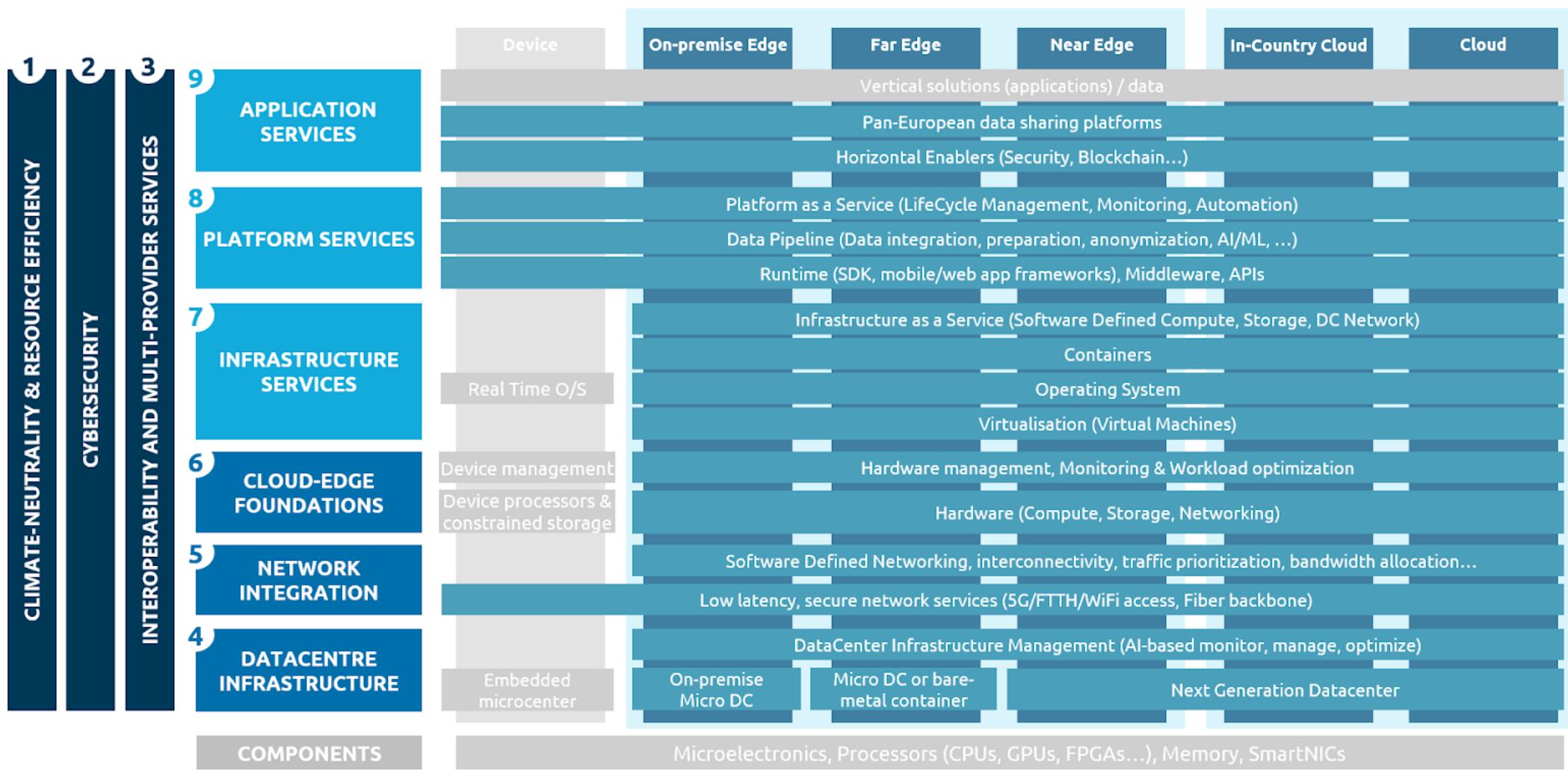
# RISE ICE Data Centre



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# Technical scope of domains covered by the next generation cloud-edge industry roadmap

Out of scope of the Next Generation Cloud-Edge technology roadmap



# RISE ICE Data Centre



ICE Connect

SERVICES PRICING HELP

Log in / Sign up



## Experimental Compute Cloud

Deploy and manage bare-metal servers or GPU VMs.



## Experimental Kubernetes Cluster

Deploy, manage and monitor workloads on GPU Kubernetes cluster using Rancher GUI.



## S3 Storage

ICE S3 is an object storage service powered by our Ceph cluster. [Click here](#) to manage your S3 storage buckets.



## OpenNebula

Build your cloud and edge spanning virtual infrastructure using IaaS powered by OpenNebula.



GitLab



Harbor



Discourse



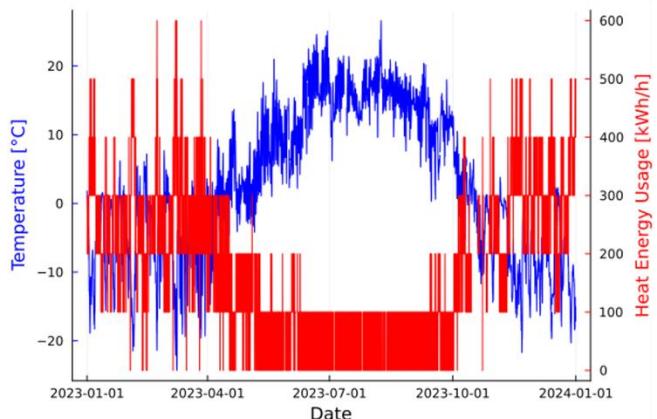
ColonyOS

RI.  
SE

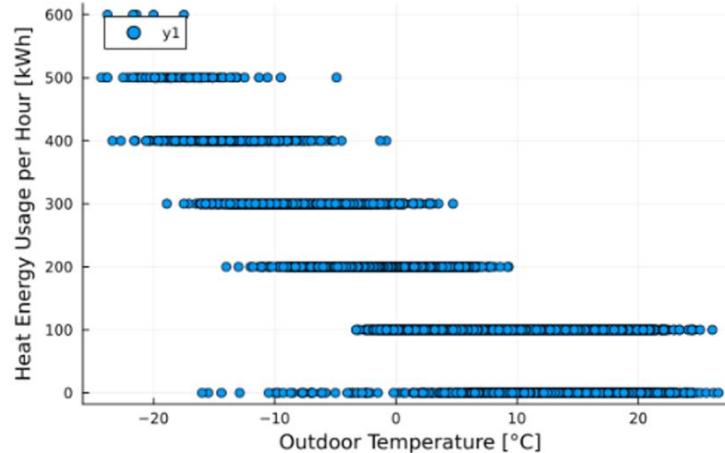
# Digital twins



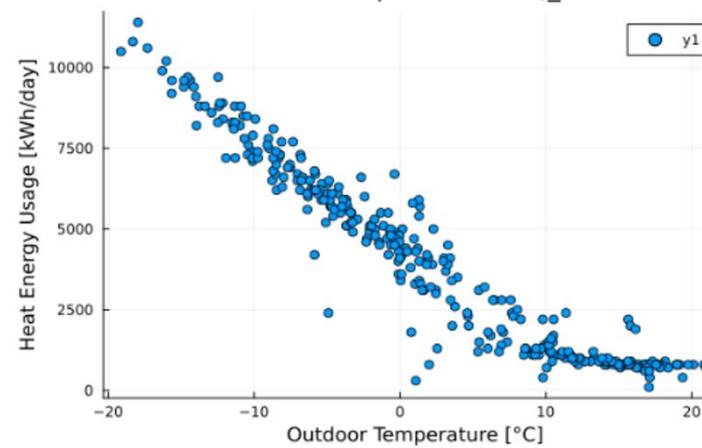
Industrial Building with RISE Pilot



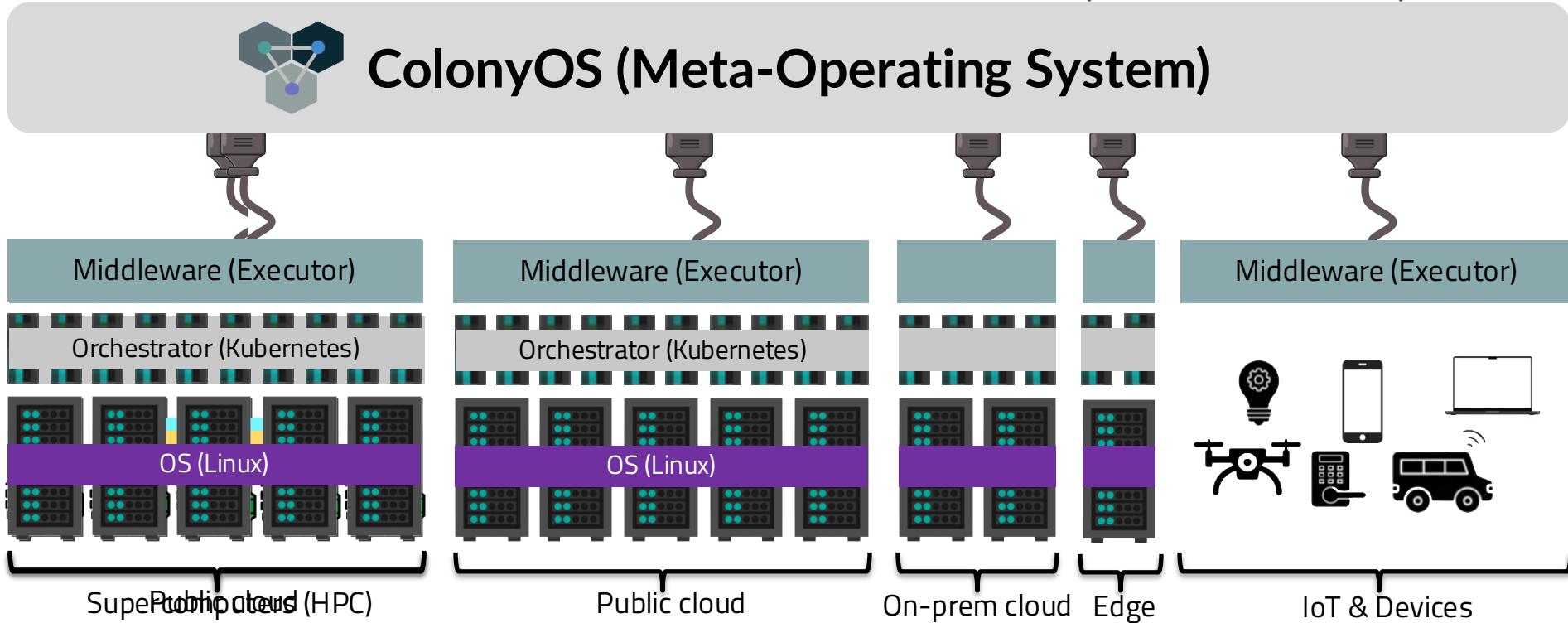
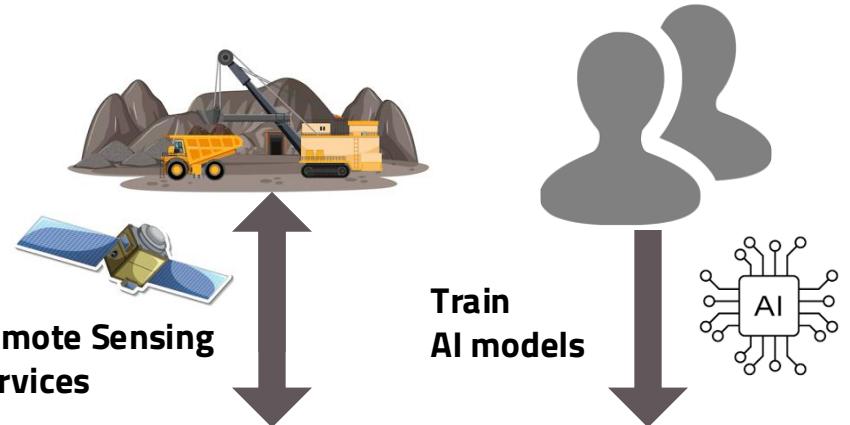
Outdoor Temperature vs Q\_kWh



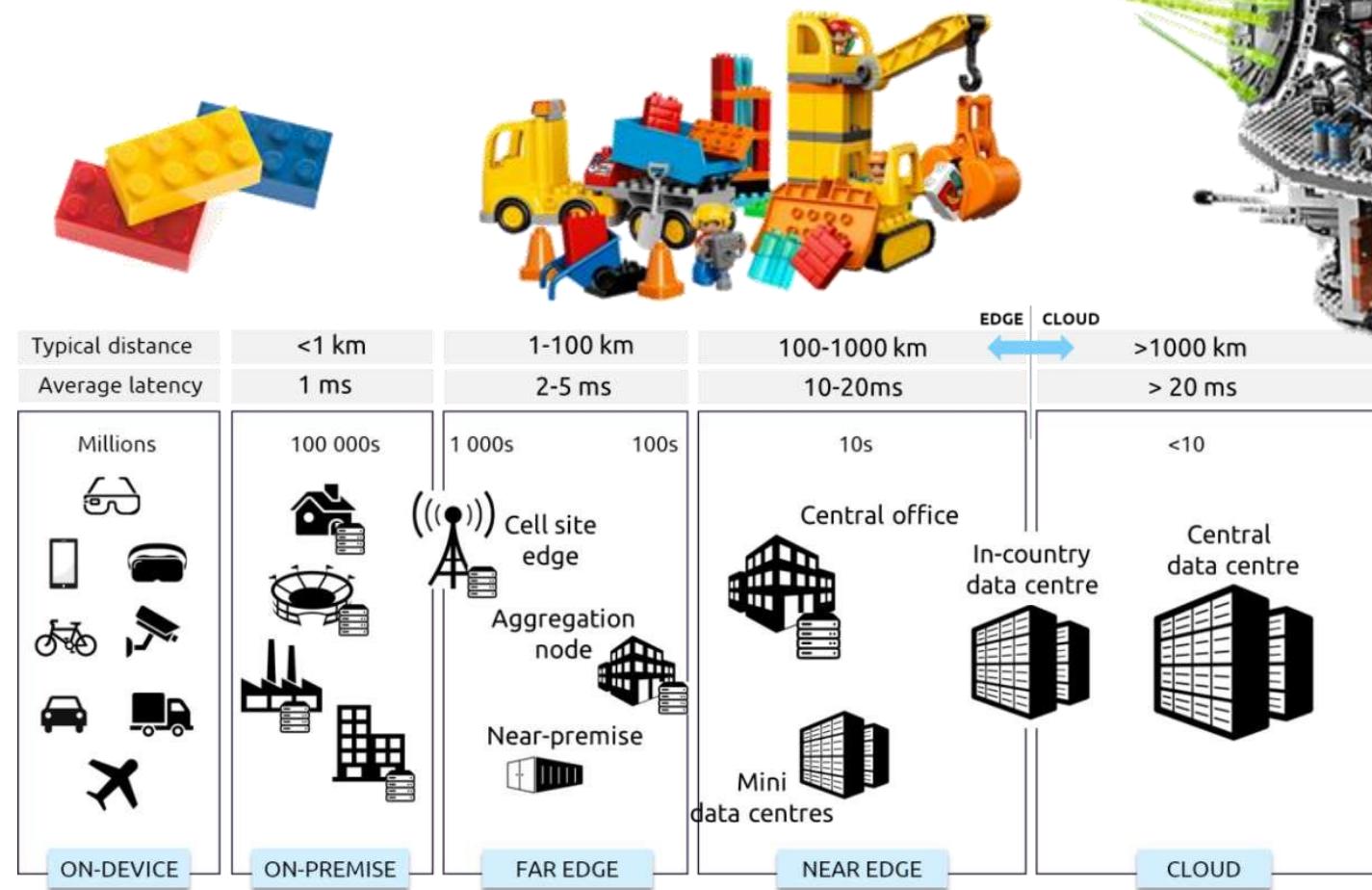
Outdoor Temperature vs Q\_kWh



# ColonyOS Meta operating system



# What is next?



Reference: European Industrial Technology Roadmap for the Next Generation Cloud-Edge Offering European Commission

# Open Compute Project

## INCUBATOR



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TECHNOLOGIES  
SYMPOSIUM

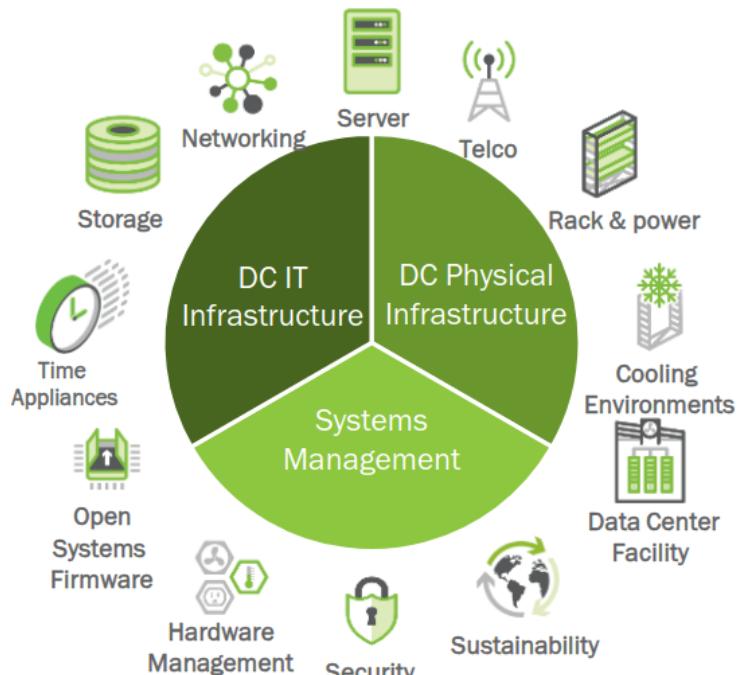


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## NEW INITIATIVES

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Evenstar  
OpenRAN

Test &  
Validation

## MARKETS

Photonics  
Chiplets

## EMERGING MARKETS

### OCP MARKETPLACE



### RECOGNITION PROGRAMS

#### Security & Facilities



#### Product





Thank you...