Experiences with the OpenAMP framework for asymmetric multi-processing

Lefteris Ntafotis Kontogiannis – FORTH

lntaf@ics.forth.gr

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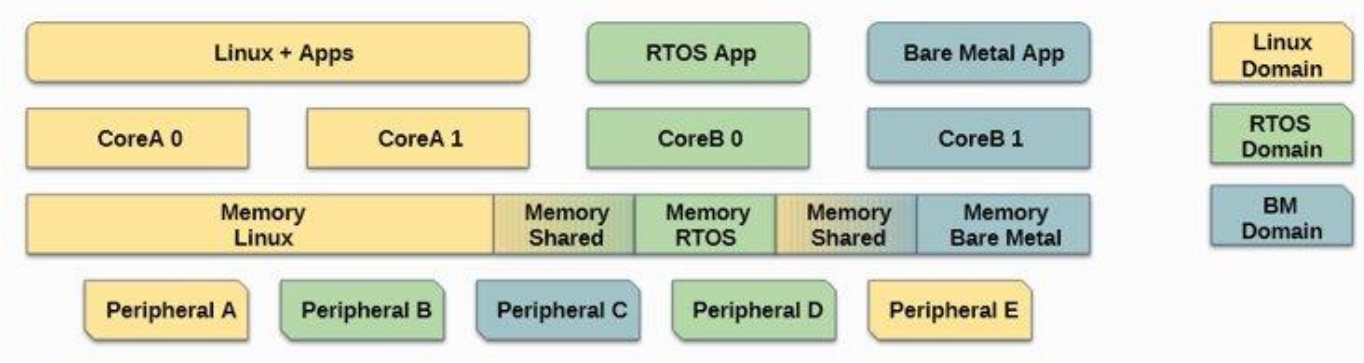
Task offload in a heterogeneous-ISA system

- RISER goal:
  - Heterogeneous-ISA task offload (ARM host + RISC-V co-processor).
  - ARM host utilizes Linux.
  - PCIe interconnect between host and accelerator as well as QSFP connections.
  - RISC-V co-processor developed through EPI and EuPilot utilizes a real time operating system (RTOS).
- Currently:
  - Attempt task offload on non-final hardware.
  - Approximate the final systems as closely as possible.
  - Understand the workflow before the systems are in place.
  - Solve any issues and complete background work required in parallel with all the hardware efforts.
  - Between the hardware efforts, our work on the EPAC chip as well as the following testing platform, capture a complete picture of the behavior in the final systems.

OpenAMP / Libmetal

- OpenAMP
  - High-level framework for inter-processor communication (RPMsg).
  - Resource sharing (virtio and vrings).
  - Remote processor management (remoteproc).
  - Built on libmetal.
- Libmetal
  - Low-level hardware abstraction layer for memory, devices and interrupts.
  - Works across heterogeneous systems.
  - APIs are inherently OS agnostic.



The Open Asymmetric Multi-Processing (OpenAMP) framework.

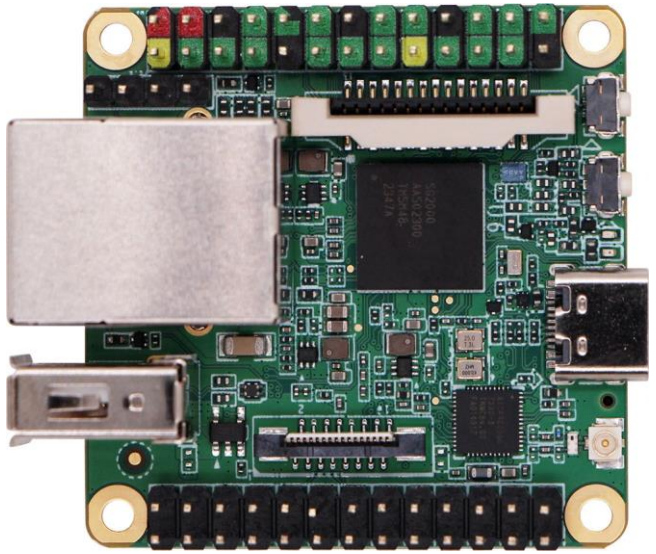
The OpenAMP Project: https://www.openampproject.org/
Libmetal: https://github.com/OpenAMP/libmetal

Testbed: Milk-V Duo S development board

- Why was this board chosen?
  - RISC – V or ARM64 "Big" core running Linux + RISC – V FreeRTOS "Small" core.
  - Open source build system that we can customize for quick iteration and tests.
- What does the internal architecture look like?
  - Mailbox driver and registers.
  - Linux can send preprogrammed commands baked into FreeRTOS.
  - Shared memory access between the two cores.
- What are we attempting to achieve?
  - Solve any potential roadblocks in the final systems ahead of time.
  - Test different ways that co-processing could be achieved in finalized hardware.

```
rtos_cmdqu {
    compatible = "cvitek,rtos_cmdqu";
    reg = <0x00000000 0x01900000 0x00000000 0x00001000>;
    reg-names = "mailbox";
    interrupts = <0x00000000 0x00000055 0x00000004>;
    interrupt-names = "mailbox";
```

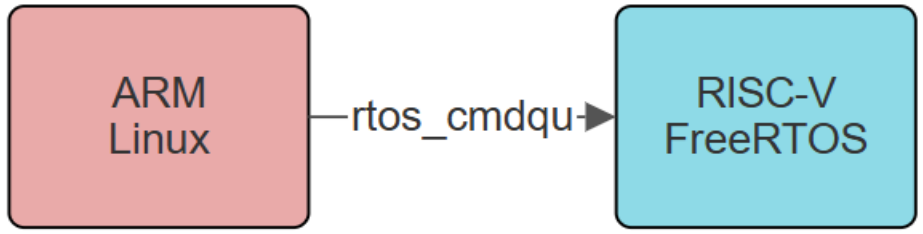
Mailbox driver as exposed by the board's device tree.



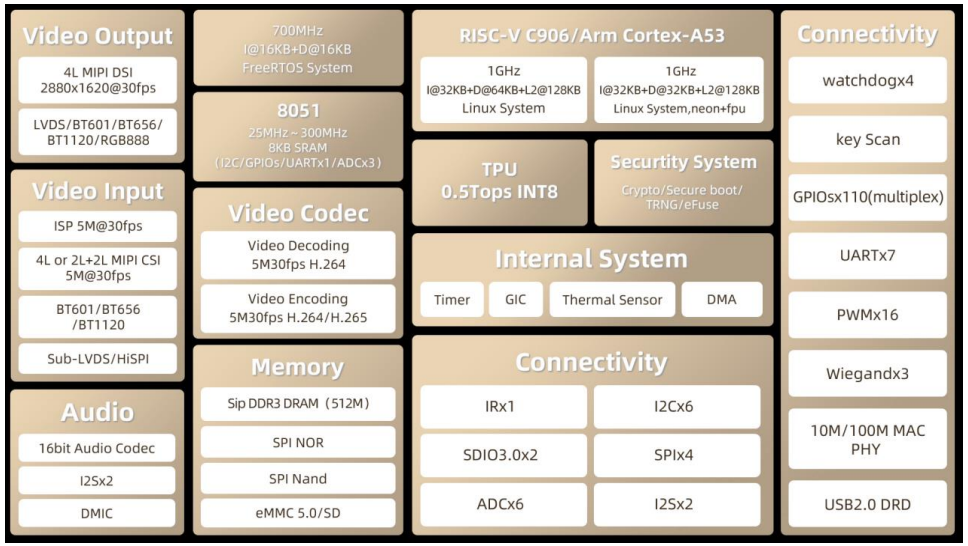
The Milk-V Duo S board.

Arm + RISC-V testbed

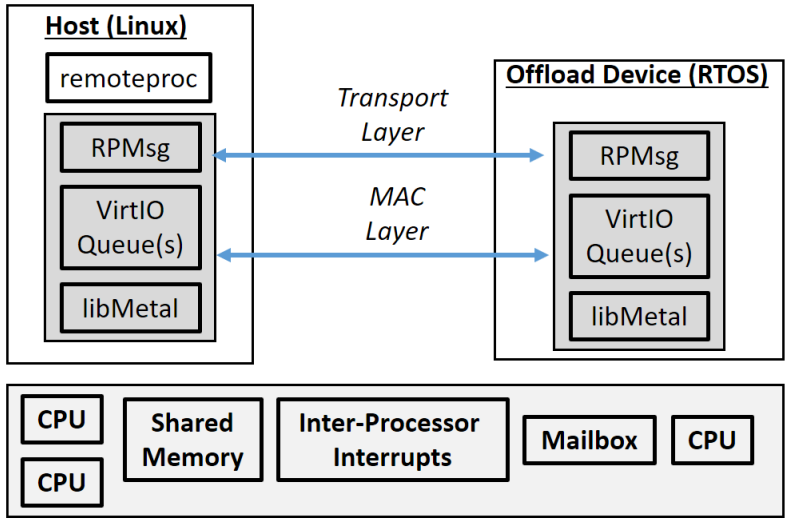
Milk-V Duo S dev. kit (Arm + RISC-V cores)
[https://milkv.io/duo-s]



ARM → RISC-V interaction, through OpenAMP (mailbox & shared memory area)



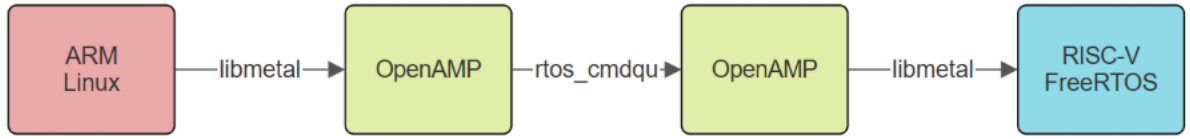
SG2000 block diagram (The SoC featured on the Milk-V Duo S)



+ upstream contribution regarding libmetal for RISC-V (incl. test-suite)

Progress thus far

- OpenAMP
  - QEMU.
  - RISC-V intra-core communication (RPMsg, vrings, shared memory).
  - ARM intra-core communication (RPMsg, vrings, shared memory).
- Libmetal
  - ARM + RISC-V mostly complete.
  - FreeRTOS implementation only partial.
  - Cross-platform testing suite upstreamed.
- Operating systems
  - Customizations to the Linux side (ARM), mostly inter-core communication.
  - Customizations to FreeRTOS.
  - Calls to custom FreeRTOS procedures from Linux.



Block diagram of our system design.

Next Steps

- libmetal small core full implementation.
  - Continue with FreeRTOS or switch to Zephyr.
    - FreeRTOS perhaps quicker to implement and test.
    - Zephyr already supports libmetal, is more versatile but more work firmware side.
- OpenAMP running on small core.
  - Requires full libmetal build and execution.
    - Zephyr also natively supports OpenAMP
- Evaluating best course for co-processing.
  - Frequent operations could be preprogrammed.
  - Binaries generated via toolchains before execution.
  - (Out of scope) Dynamic binary creation, JIT compilation, binary translation.

Thank you for your attention.

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