DARE: Digital Autonomy with RISC-V in Europe

RISC-V Summit Europe 2026 | 12th June, 2026

Advancing RISC-V Adoption in HPC and Cloud Environments

Teresa Cervero (BSC) | VEC Pathfinding Technical Coordinator

Paul Carpenter (BSC) | Software Technical Area Coordinator

Co-funded by the European Union

EuroHPC Joint Undertaking

The DARE project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No 101202459. The JU receives support from the European Union's Horizon Europe research and innovation programme and Spain, Germany, Czechia, Italy, Netherlands, Belgium, Finland, Greece, Croatia, Portugal, Poland, Sweden, France and Austria. Funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or the co-funding granting authority. Neither the European Union nor the granting authority can be held responsible for them.

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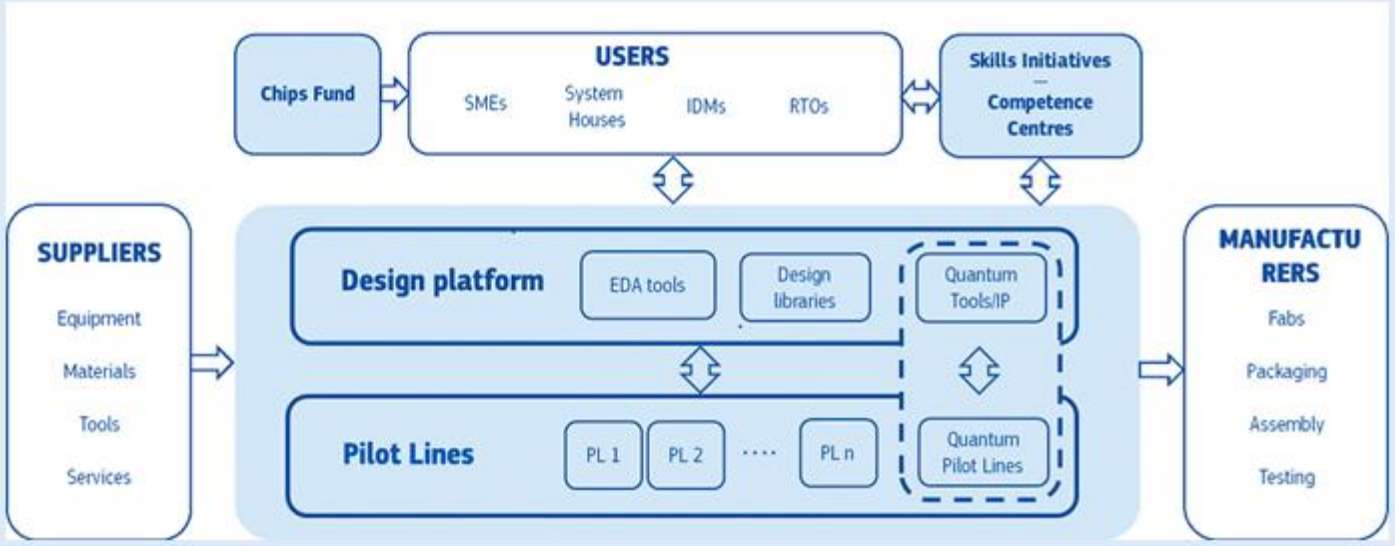
A bit of context:

What? → Why? → How?

RISC-V® in Europe | European Commision

Sustainability	Circular economy – **Modernise industry** to green transition
Autonomy	Avoid one-sided **dependencies**
Competitiveness	Scale up start-ups in **innovation-friendly** ecosystems
Sovereignity	**Modernize education**, training and reskilling in all areas



✓ *RISC-V ISA plays a central role on EU's technology strategy*

Digital Europe | European Chips Act
1,98 B€

Horizon Europe | Technology
900 M€

Connecting Europe
200 M€

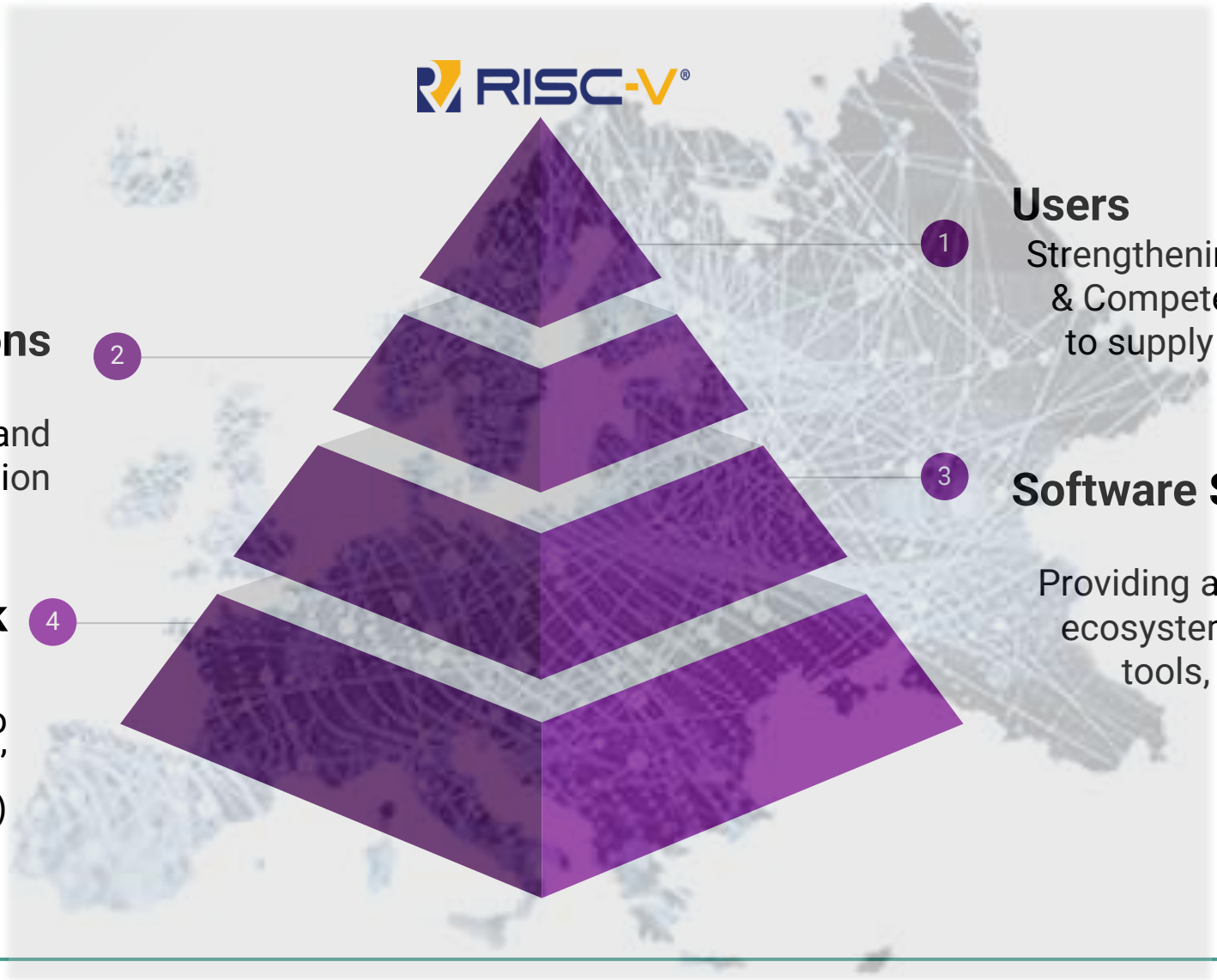
EuroHPC Joint Undertaking
2 B€

European Commission

RISC-V in Europe

EuroHPC Joint Undertaking

Chips JU



Users

Strengthening users skills & Competencies in HPC, to supply market needs

HPC & AI Applications

Characterization, porting, and optimization

Software Stack

Providing a complete EU SW ecosystem (i.e. algorithms, tools, models, libràries)

Hardware Stack

Creating EU HW ecosystem to supply modern workloads' demands (PPA)

RISC-V® | EuroHPC vision

EuroHPC Joint Undertaking

EU Goal: Autonomy in Strategic Processing Technologies

*Our **ambition:** by 2030*

- *The production of cutting-edge and sustainable semiconductors in Europe including processors is at least **20% of world production** in value*
- *Manufacturing capacities below **5nm** nodes aiming at 2nm*
- ***Energy efficiency** 10X more than today*

✓ ***RISC-V ISA plays a central role on EU's technology strategy***

RISC-V® | EuroHPC vision

EuroHPC Joint Undertaking

EU Proposed Roadmap: 2024 - 2030

MANUFACTURING	**2 nm** and below technology and production facilities
DESIGN Short term (2024-26)	**First RISC-V IPs** • **Build on EPI** efforts on ARM-based processor • From test chips to **TRL 9** • EuroHPC exascale systems as first customer and scale to **embedded**
Medium term (2026-28)	New RISC-V architectures • **Complement the work of EPI** and Pilots on RISC-V with stand-alone competitive GPPs and GPUs • Collective effort building on **EU R&D** in low power, security,…, • EuroHPC **post-exascale** system as first customer
Long term (2028-)	**Post-exascale RISC-V** systems based on EU R&D, manufactured in EU.

RISC-V® | EuroHPC vision

EuroHPC Joint Undertaking

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Long term (2028-)	**Post-exascale RISC-V** systems based on EU R&D, manufactured in EU.

RISC-V® | EuroHPC vision

EuroHPC Joint Undertaking

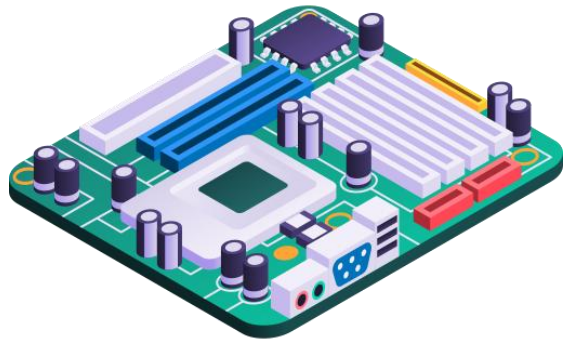
- Towards the **next-gen** of EU **HPC technology** based on RISC-V
- **Partnerships** (Academia & industry): a key piece
- **Open-standards** to design & develop locally → impact globally
- Towards **European post-Exascale** supercomputer using RISC-V
  - RISC-V **accelerators**
    - Traditional HPC workloads
    - New Data Analytic workloads (Digital Twins, AI models…)

dare in a nutshell

Why? **Contributing** to the EU Tech. Autonomy

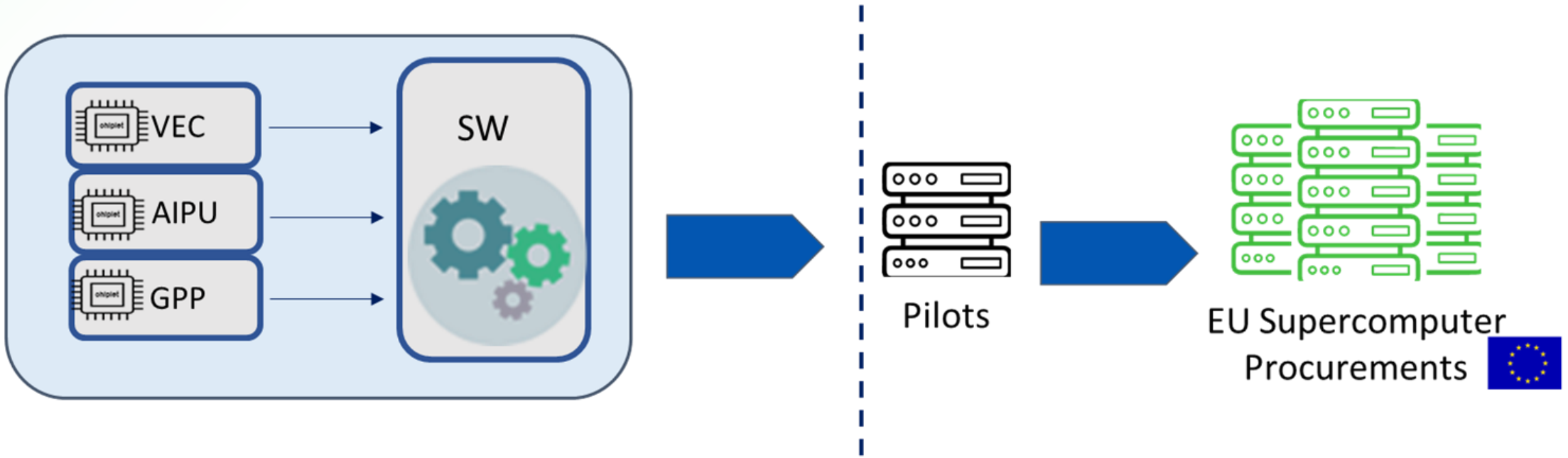
How? Building a **complete HW & SW ecosystem** based on RISC-V

dare in a nutshell

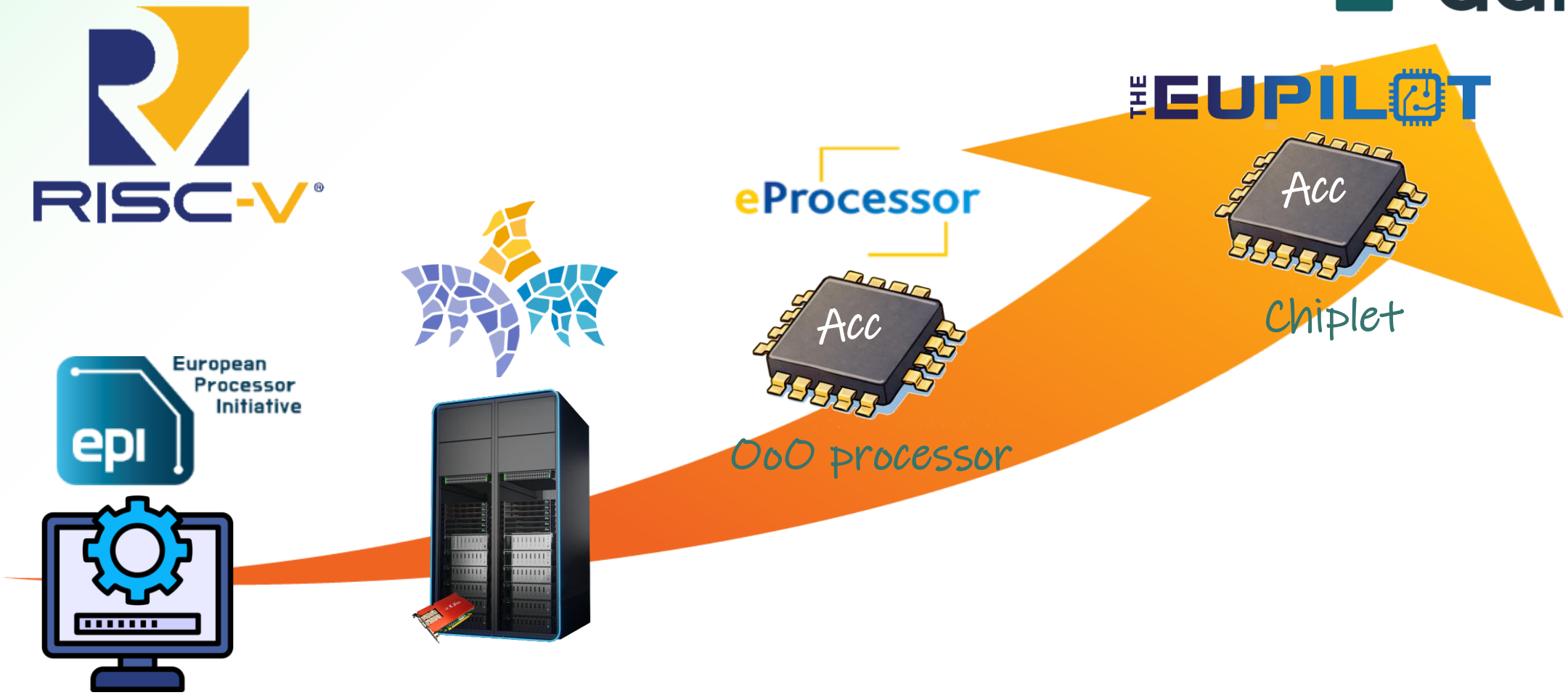


Why? **Contributing** to the EU Tech. Autonomy

How? Building a **complete HW & SW ecosystem** based on RISC-V



dare 's enablers



dare 's enablers

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RISC-V®

THE EUPILOT

ePProcessor

Acc

Acc

Chiplet

European Processor Initiative

epi

OoO processor

- Tools
- Know-how
- Competences

R&D

Industrial

DARE SGA1 Project Structure - Technical Areas

BSC
Coordination & Roadmap Technical Area

Openchip
VEC
Vector Accelerator
Technical Area

Axelera AI
AIPU
Inference Accelerator
Technical Area

Codasip
GPP
General Purpose
Processor Technical Area

imec
Integration and Prototyping technical Area

JSC & BSC
Shared Applications & Software Technical Area

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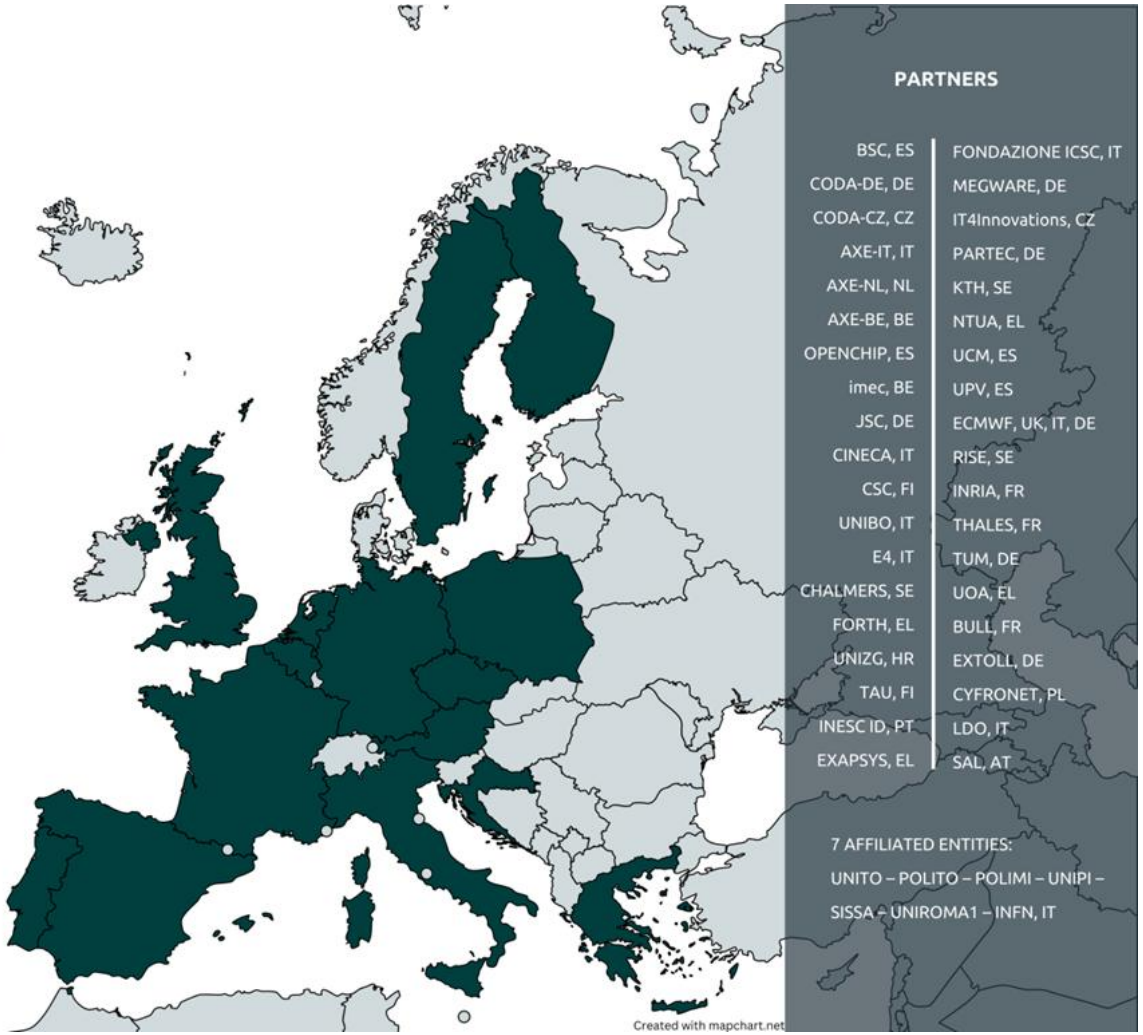


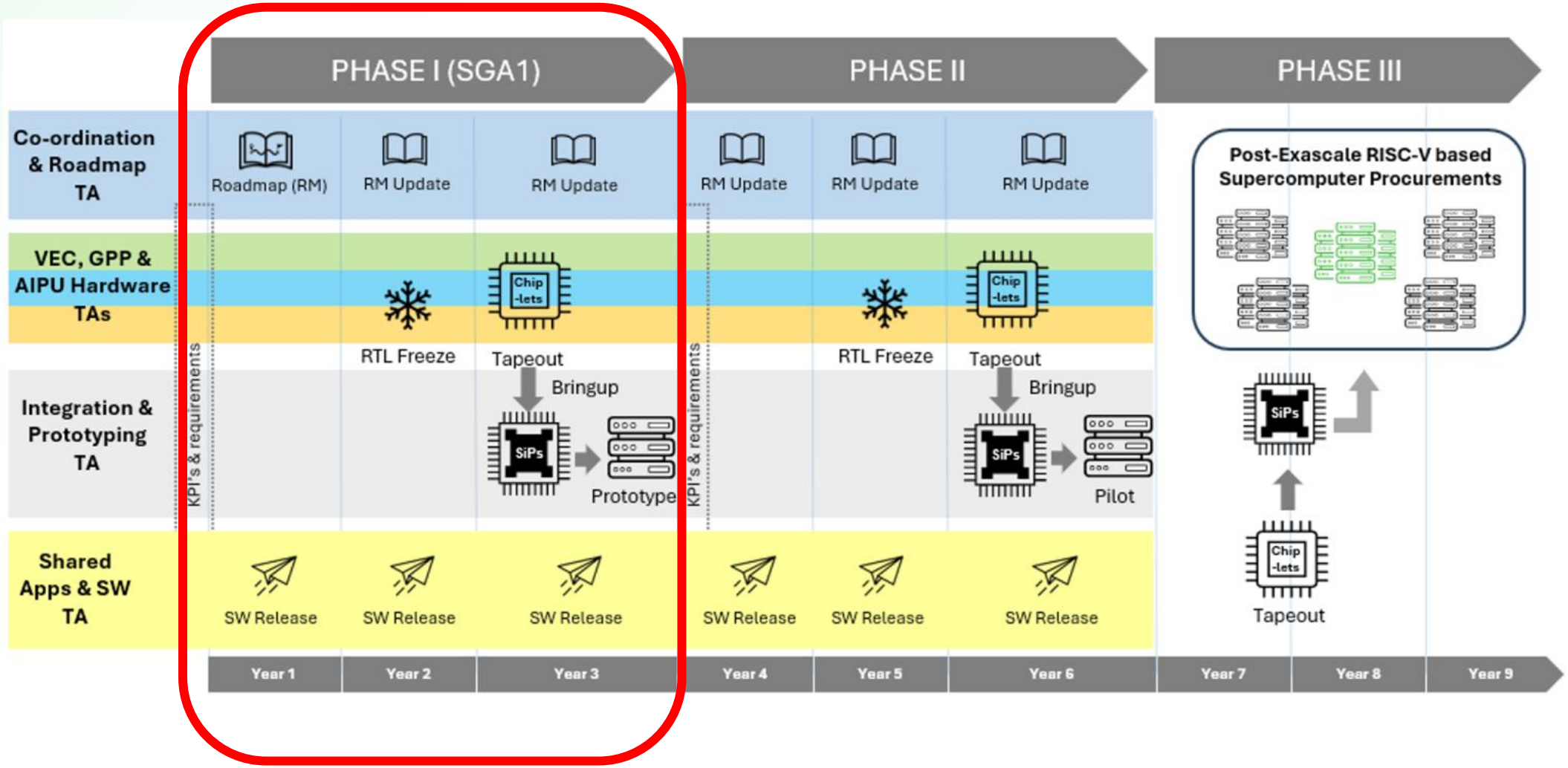
29 work packages

38 partners and 7 affiliated entities

240 MEUR
(50% EU+ 50% Member States)

3 years

DARE SGA1 and future phases



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VEC Pathfinding

Co-funded by the European Union

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VEC TA partners

RISC-V based HPC accelerator using long vectors, matrix multiplication extension and large memory bandwidth.

openchip

Chiplet → SiP → PCI Card
productisable
reasonable tech node
competitive

R&D
Verified IP
ready for tapeout
basis for next DARE phase

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

CHALMERS UNIVERSITY OF TECHNOLOGY

FORTH INSTITUTE OF COMPUTER SCIENCE

EXTOLL latency matters.

Faculty of Electrical Engineering and Computing

Università di Pisa

Politecnico di Torino

Sapienza Università di Roma

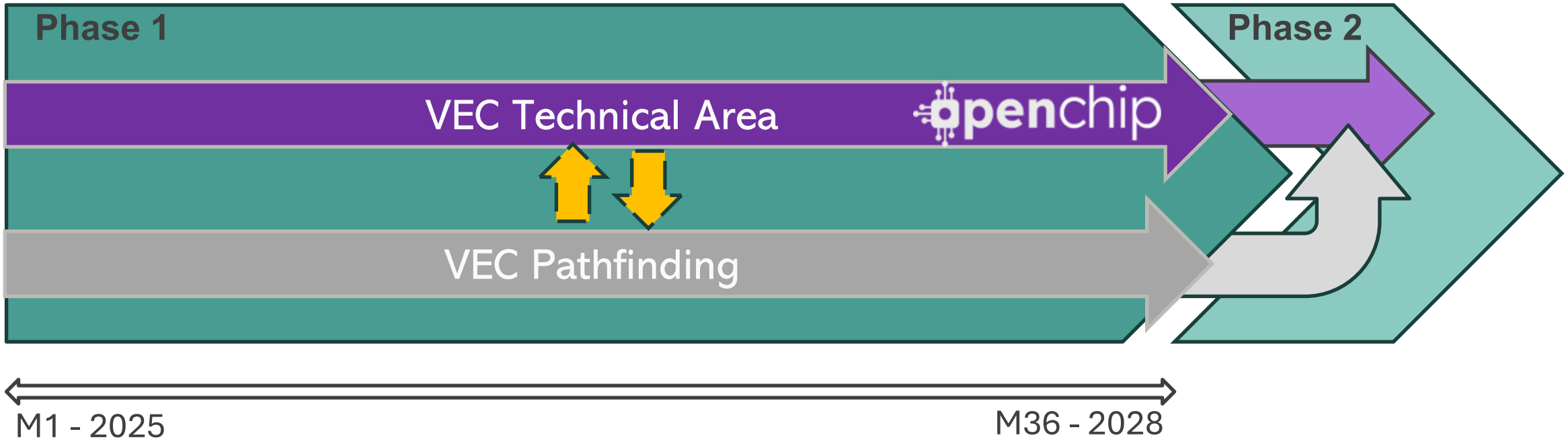
VEC Pathfinding: Overview and Objectives

Main Objectives

Objective 1. Build an architecture that balances future HPC & AI apps for HPC workloads.

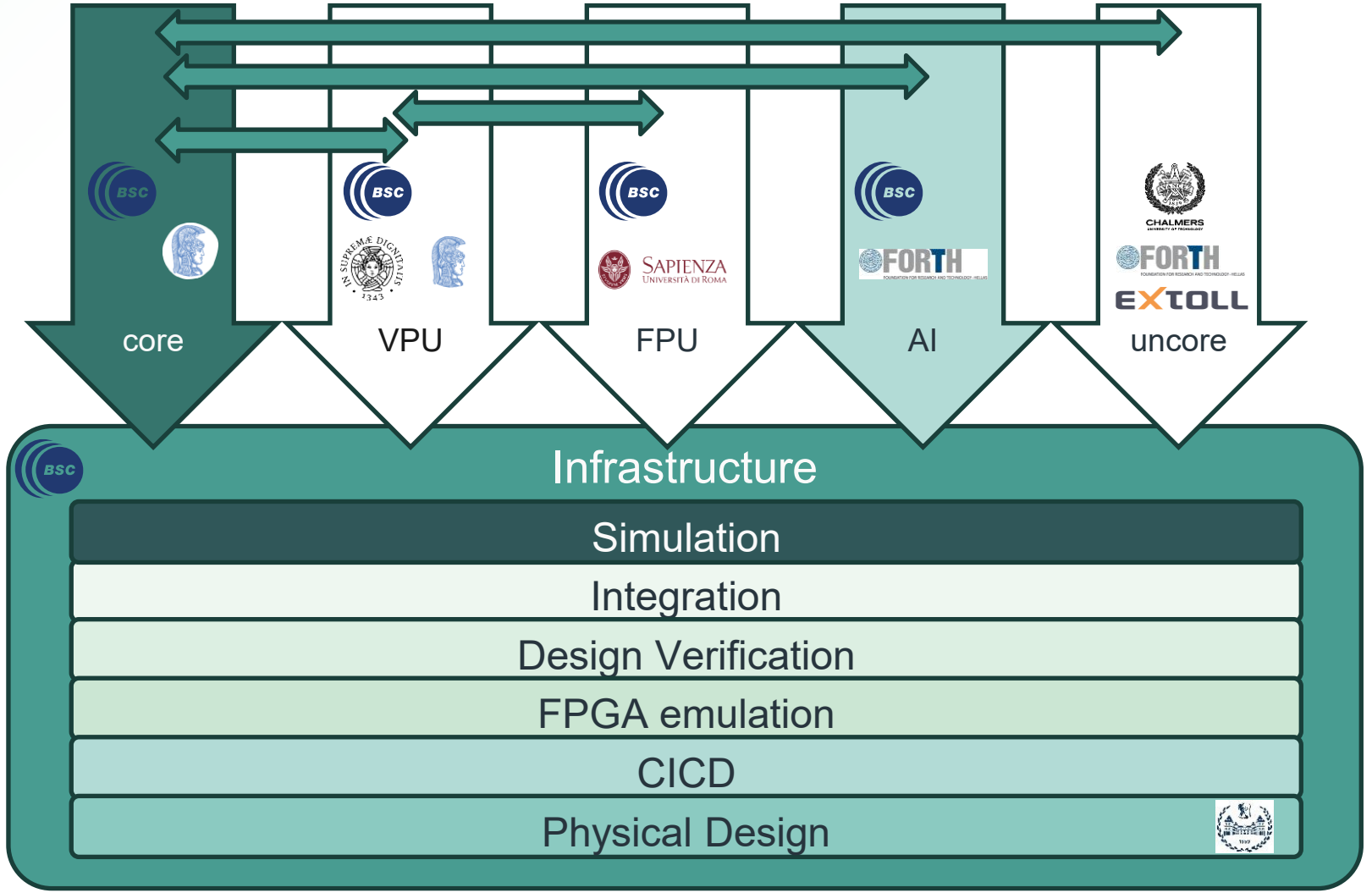
Objective 2. Close interaction between VEC Pathfinding & SW TA to extract apps' requirements.

Objective 3. Develop components and technologies to contribute to the Phase 2 of the project.

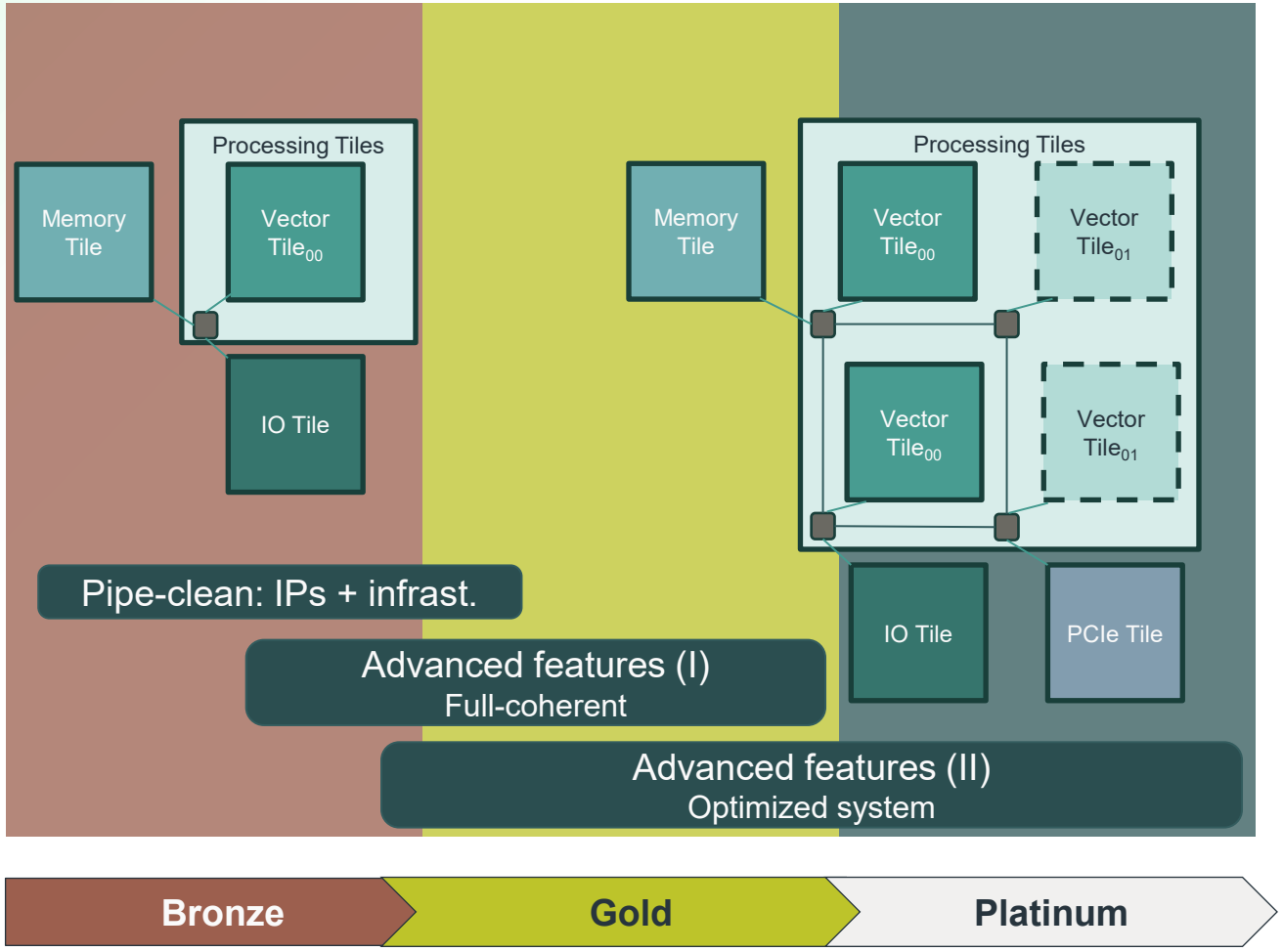


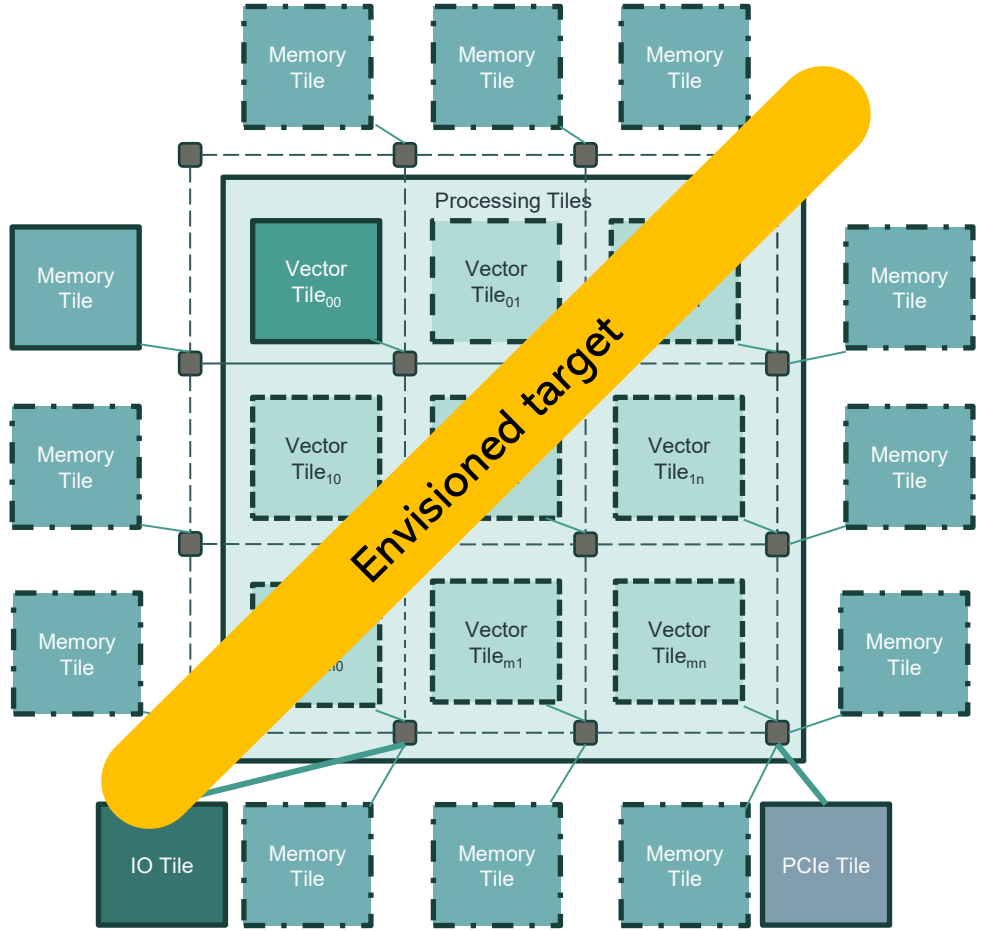
VEC Pathfinding: Partners & Tasks

- BSC
- CHALMERS
- EXTOLL
- FORTH
- ICSC-POLITO
- ICSC-UNIPI
- ICSC-UNIRM
- UOA



VEC Pathfinding: life time evolution





SW TA: Shared Software

Paul Carpenter

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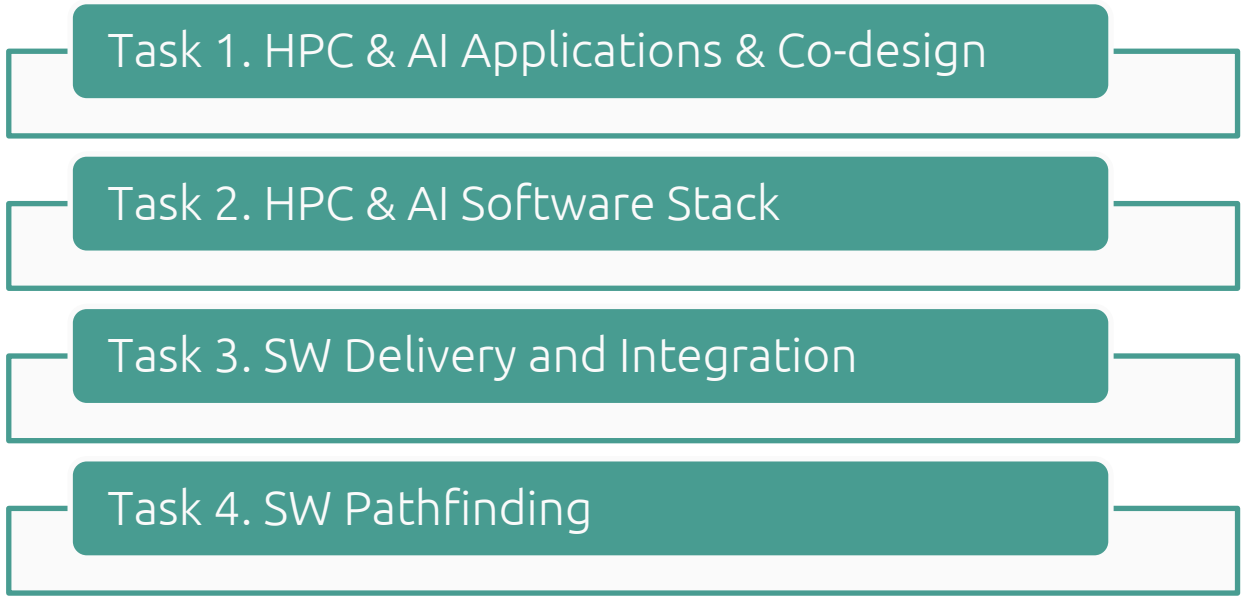
SW TA overview and objectives

Main Objectives

Objective 4. Analyse & port **7** critical EU HPC and AI Apps used for HW/SW co-design.

Objective 5. Develop & integrate a full optimised, competitive & sustainable HPC/AI SW stack for the HW.



SW TA partners

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Applications and software stack

DARE will …

- Build on European strengths in HPC and AI apps and SW stack
- Perform HW/SW co-design for the Phase 1 & Phase 2 DARE designs
- Optimize apps and SW stack for the three DARE devices
- Contribute to Open Source SW implementations available for RISC-V
- Leverage RISC-V Software Development Vehicles (SDVs) from day one

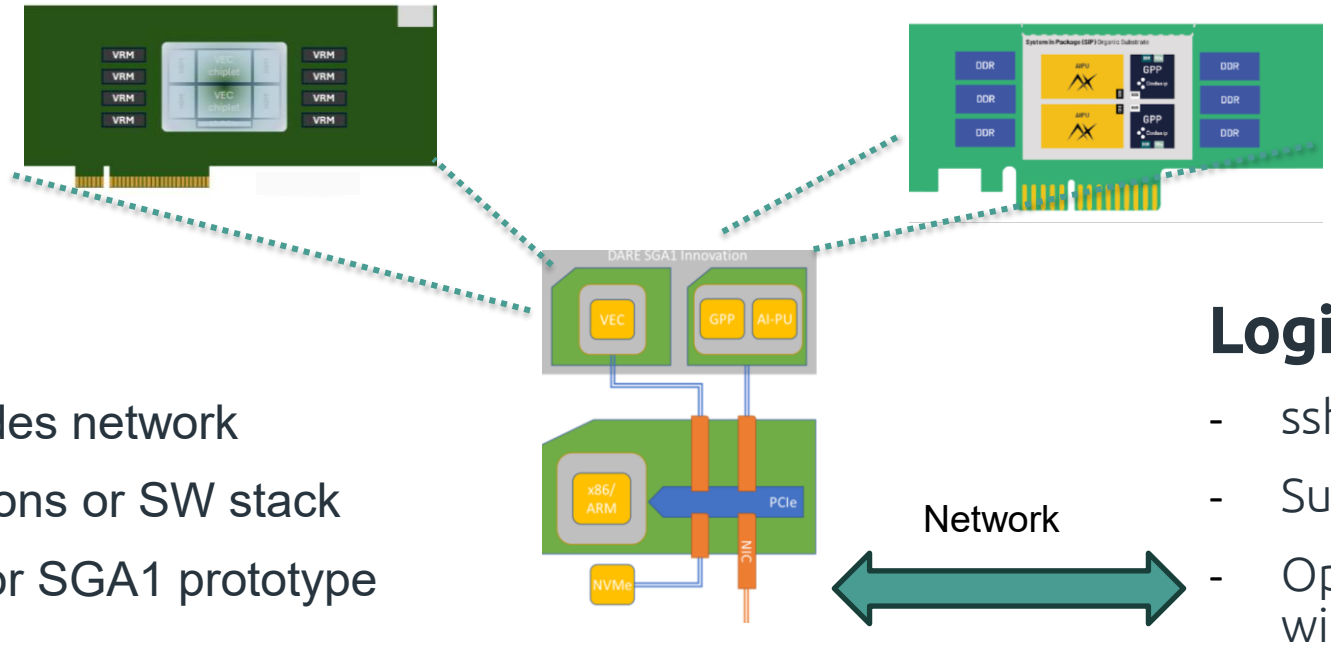
Software execution model for DARE SGA1 prototype (SDVv4)

VEC

- Runs Linux
- Runs main: application & SW stack
- Hosts MPI processes

GPP + AIPU

- GPP runs Linux
- GPP runs main: application & SW stack
- GPP hosts MPI processes



x86 host

- Boots node and provides network
- Does not run applications or SW stack
- Temporary measure for SGA1 prototype

Login node

- ssh access
- Submit jobs
- Optional: "beefy" to help with cross-compilation

Co-design applications

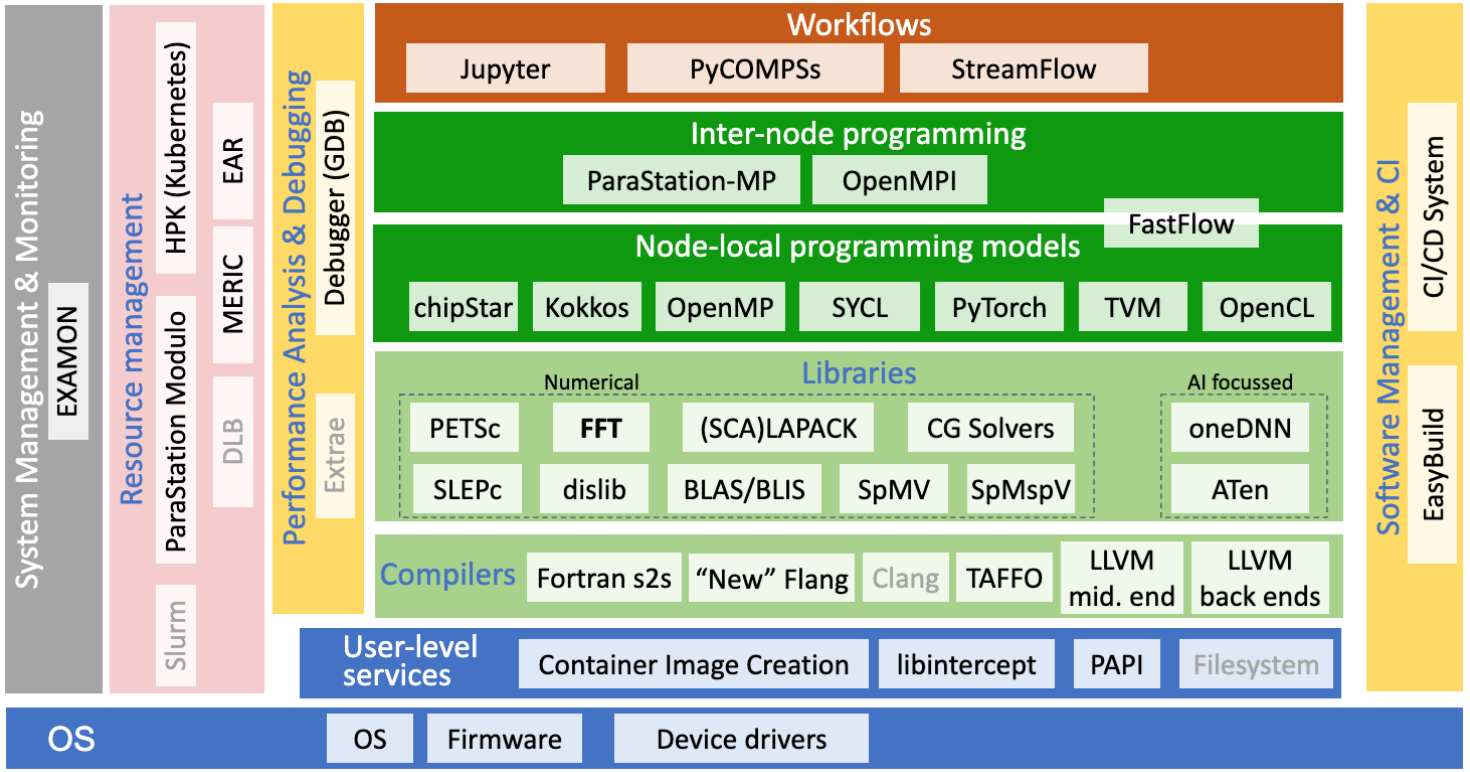
- Applications represent significant portion of workloads on European HPC centres
- Owner / significant contributor in the consortium
- Open source

Application	Description	VEC	AIPU	GPP	Notes
IFS	Weather prediction	x	c	x	Fortran
NEMO	Ocean model	x		x	Fortran
GROMACS	Biomolecular simulation	x		c	C++, optimize **SYCL** version
Quantum ESPRESSO	Quantum chemistry	x		c	Fortran
Alya + PyLOM	Air quality and pollution		x	x	Alya: Fortran, PyLOM: deep NN inference
LLMs	AI language model	x	x	c	Inference, possibly training
SuSy	AI synthetic content detection		x	c	CNN inference
PhysiBOSS	Agent-based biological model	c	c	c	C++, for co-design only

x: Co-design, ported and optimized c: Co-design input only

Integrated software stack for DARE devices

- Integrated and optimized SW stack
- Based on existing standards
  - MPI, OpenMP, Fortran, BLAS, SYCL, PyTorch, etc.
- Focus in SGA1 on
  - Compilers, especially Fortran
  - Autovectorization and OpenMP
  - Optimized libraries for both HPC and AI
  - MPI supporting both MPI families: PS-MPI/MPICH and OpenMPI



Software development vehicles (SDVs)

VEC GPP AI

SDVs are critical to the success of the SW TA

- SDVs to be usable by SW partners: ssh access, batch scheduler, environment modules, etc.
- Builds on BSC's infrastructure and experience from EPI, BZL and EUPILOT

From day 1: Partners already using **off-the-shelf RISC-V platforms** (some with RVV)

- Port SW to RISC-V, use RVV vector instructions

From M6: **Instruction-accurate functional emulators** (gem5, QEMU)

- Use specific instructions, e.g. matrix, AIPU data formats

From M15: **Scale-out simulator**

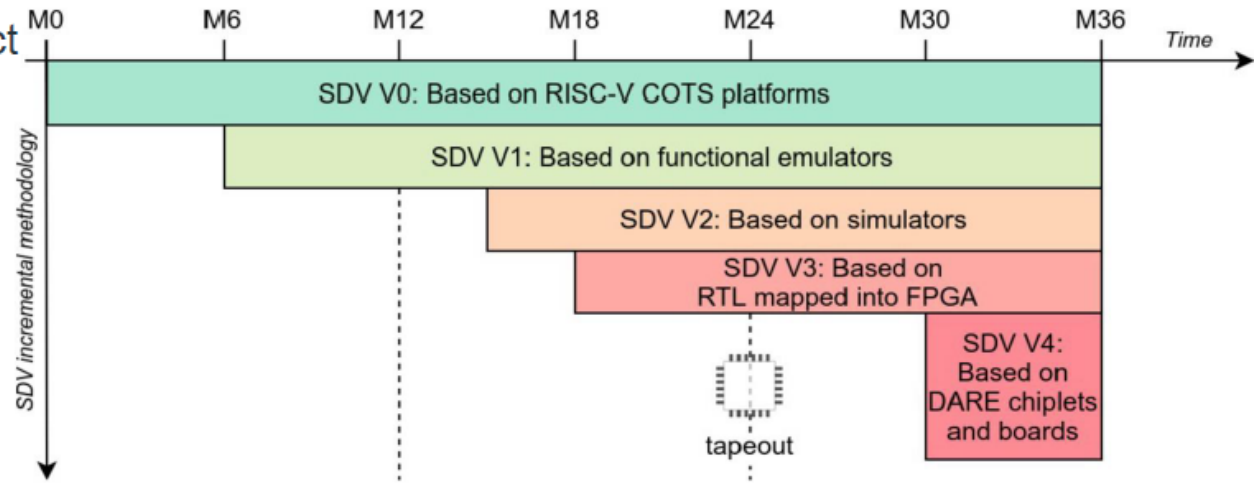
- Performance analysis with multiple devices and interconnect

From M18: RTL mapped to **FPGAs**

- Faster performance analysis at smaller scale

From M30: **Multi-node physical prototype**

- Demonstrate and evaluate project results



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Application-driven Co-Design

VEC GPP AI

Continuous co-design throughout the project

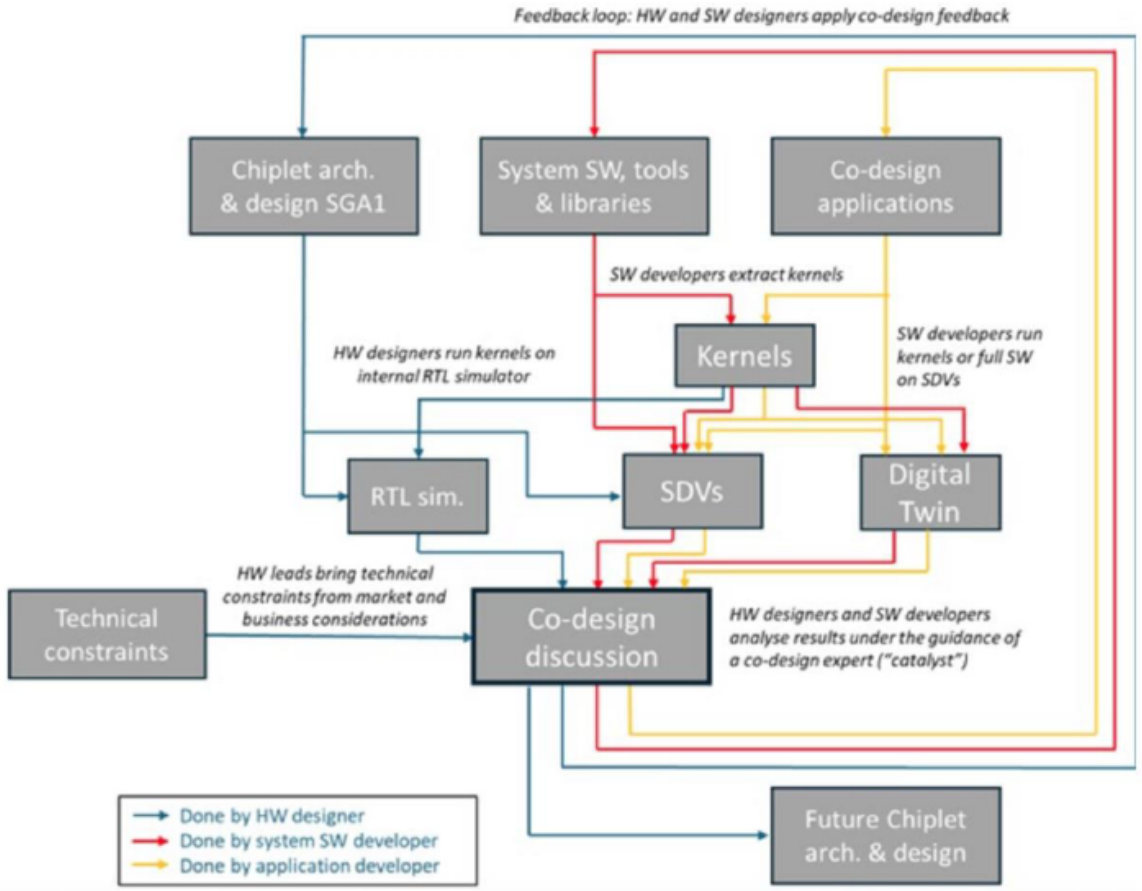
- For M6: devices and prototype to be developed in SGA1
- After M6: operation-ready devices and systems in SGA2

Close collaboration with application and SW stack

- Collect, combine and consolidate co-design inputs
- Consolidate and pass down co-design information

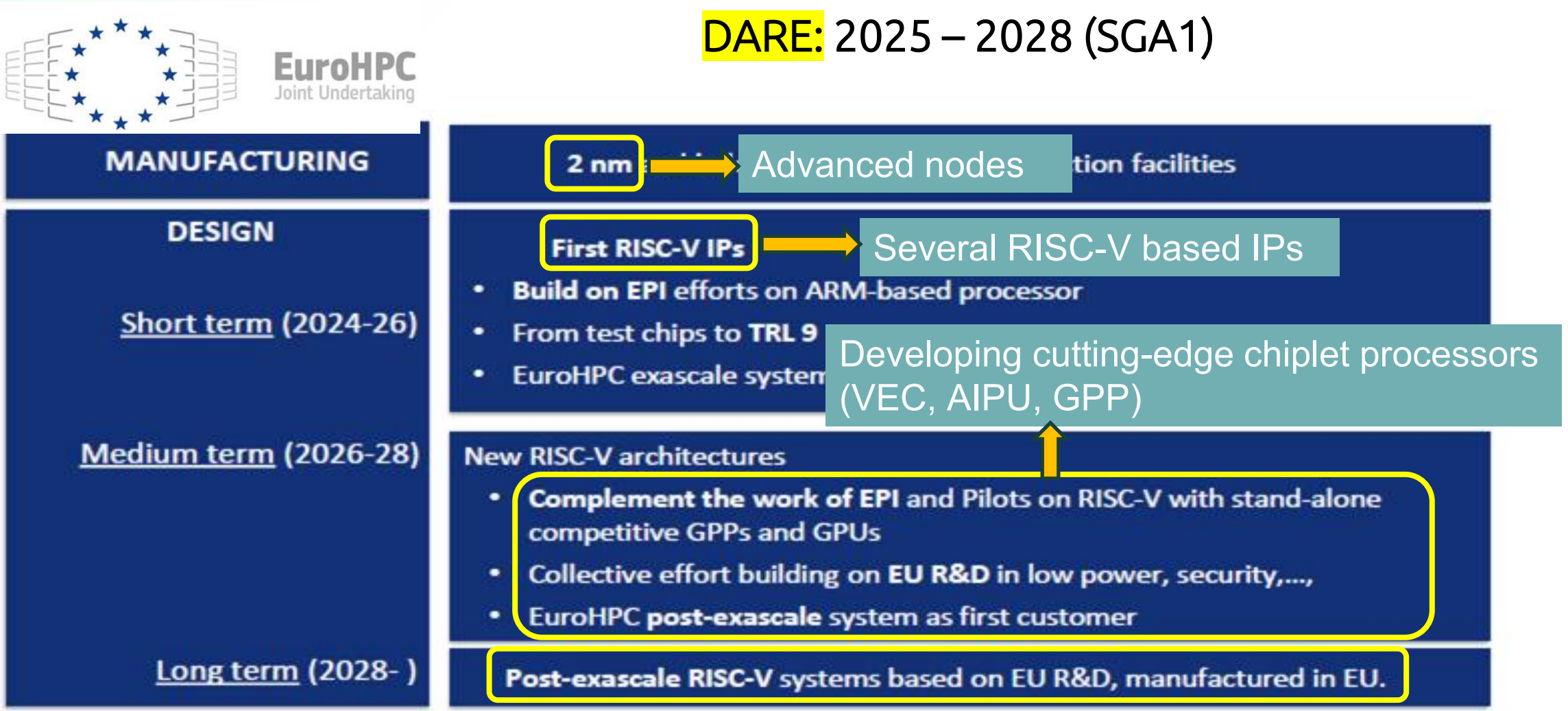
Close interaction with HW and integration

- Facilitate effective information flow in both directions
- Help bridge gaps between HW and SW viewpoints



Conclusions

DARE: 2025 – 2028 (SGA1)



Thank you!

https://dare-riscv.eu/home/

/dare-risc-v-in-europe

@dare-eu.bsky.social

@dare_euproject

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GPP TA: General Purpose Processor

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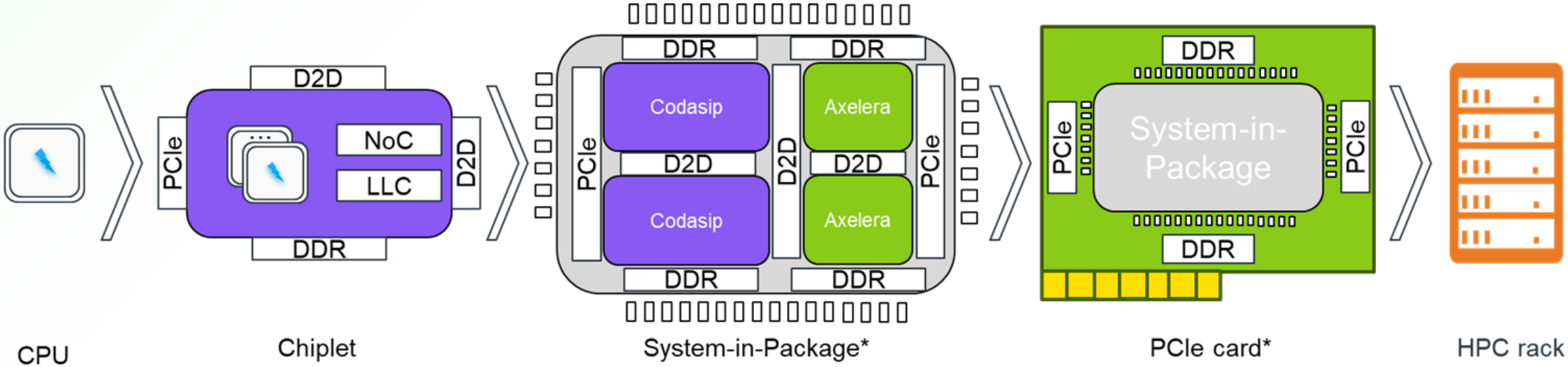
GPP TA objectives

- High-performance, configurable and customizable **OoO RISC-V IP core**
  - SW/ HW co-design
- **Chiplet** design and **SiP** integration
  - **GPP** chiplets for HPC apps (Codasip)
  - **AIPU** chiplets for Inference (Axelera)

- Full **SW stack**
  - Middleware, OS porting, compiler
  - Compute libraries optimizations
  - Software Development Vehicles (SDVs)



* Axelera + Codasip

GPP TA partners

Codasip

HW

ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

HELLENIC REPUBLIC
National and Kapodistrian University of Athens
EST. 1837

SAPIENZA UNIVERSITÀ DI ROMA

Tampere University

Inria

BSC

CHALMERS UNIVERSITY OF TECHNOLOGY

SW and Applications

JÜLICH Forschungszentrum

ECMWF

inesc id lisboa

BSC

VŠB TECHNICKÁ UNIVERZITA OSTRAVA | IT4INNOVATIONS NÁRODNÍ SUPERPOČÍTAČOVÉ CENTRUM

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AIPU TA: Inference Accelerator

Co-funded by the European Union

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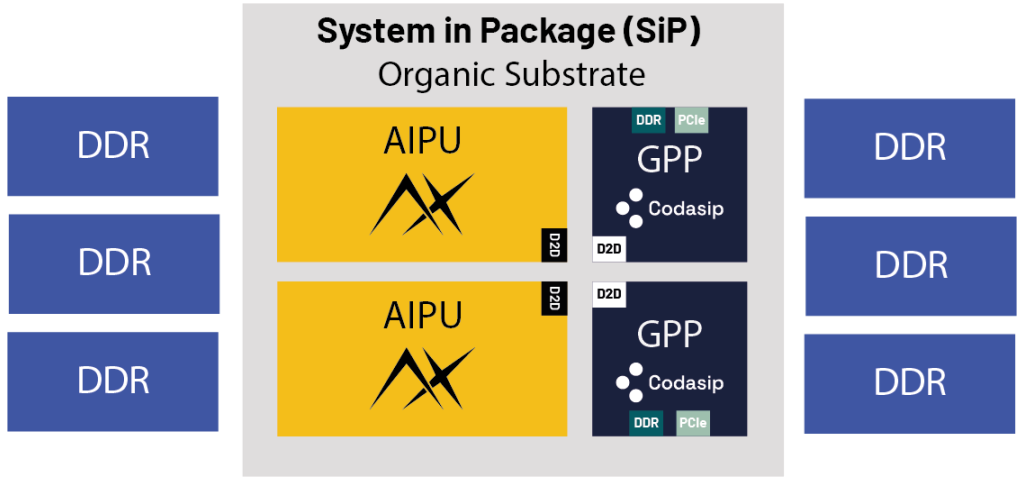
AIPU TA objectives

- Development of a **high-performance, high-energy-efficiency and scalable AI Inference chiplet**
  - **AI accelerated HPC** (weather models, materials discovery, search requests, PINNs etc.)
  - **Large-scale neural networks, i.e., Generative and Foundation models**
- AI TA and the GPP TA will build a complete **system-in-a-package** (SiP) that includes:
  - AIPU chiplet(s) for AI inferencing
  - GPP chiplet(s) for classical HPC workloads
- Develop a complete **compiler and software stack** based on the RISC-V architecture and Axelera AI's infrastructure

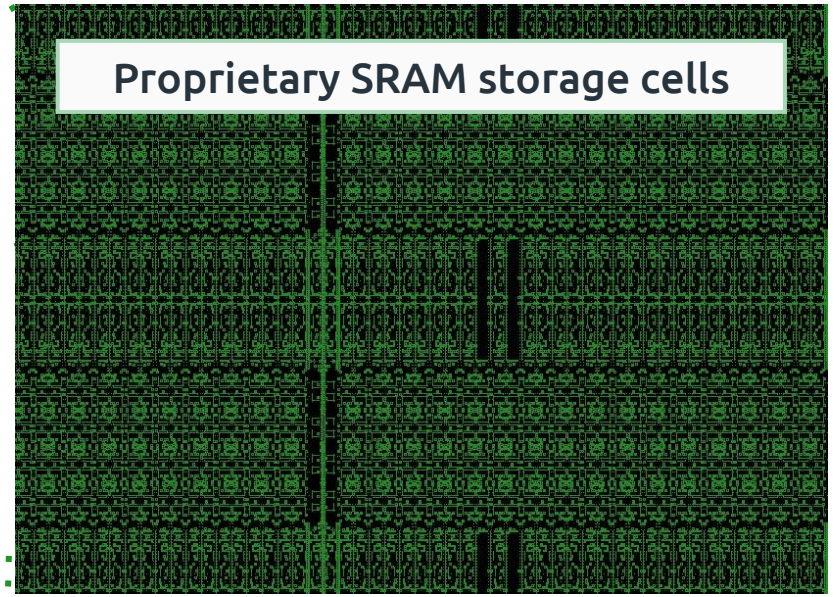


The number of chiplets in the SiP is for illustration purposes only. The exact ratio of AIPU to GPP chiplets is yet to be determined.

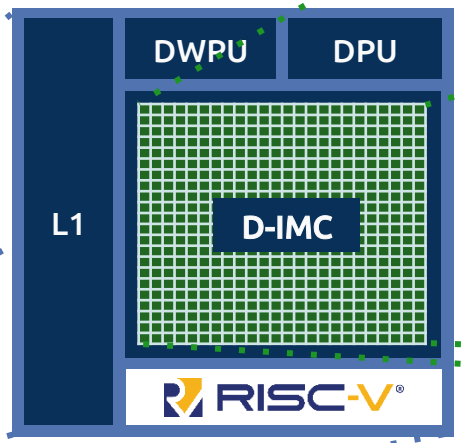
AXELERA
ARTIFICIAL INTELLIGENCE

Axelera AI's Digital-IMC-based Inference Accelerator

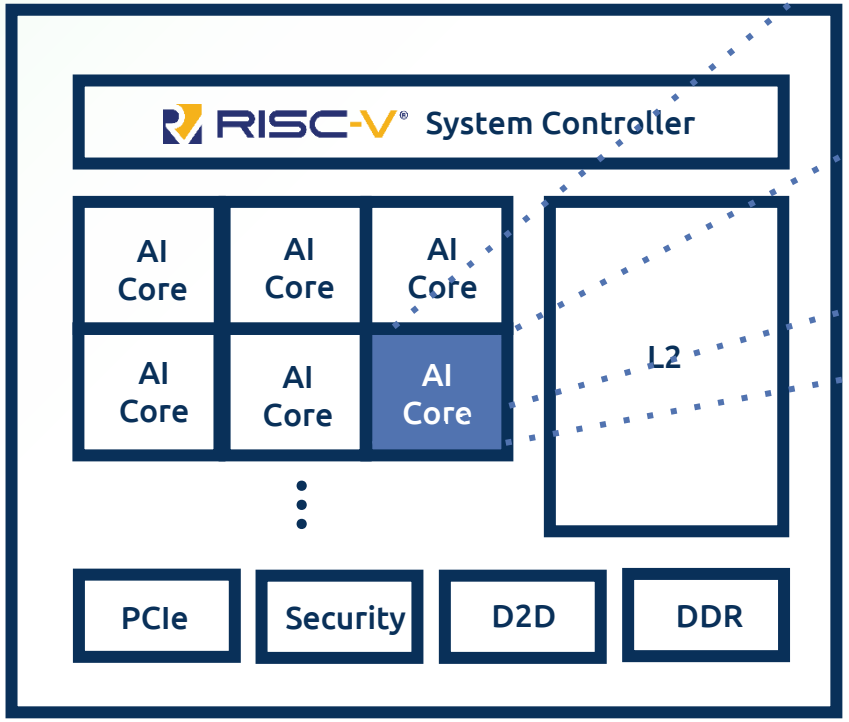
Digital-IMC



AI Core



AI Processing Unit



AXELERA ARTIFICIAL INTELLIGENCE

High throughput
high energy efficiency
scalable architecture

- Interleaved weight-storage and compute units in a highly dense fashion
- Immune to noise and memory non-idealities affecting analog IMC precision
- Accumulation in full precision with minimal loss of neural network accuracy
- Technology commensurate with CMOS scaling to low lithography nodes

AIPU TA partners

AXELERA
ARTIFICIAL INTELLIGENCE

HPC and AI Applications

BSC
CYFRONET
RI.SE
CSC
JÜLICH Forschungszentrum
Tampere University

HW

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA
HELLENIC REPUBLIC
National and Kapodistrian University of Athens
EST. 1837
PULP
Parallel Ultra Low Power
CAL@DI
ICSC
Centro Nazionale di Ricerca in HPC, Big Data and Quantum Computing
INFN

SW

POLITECNICO
MILANO 1863
LEONARDO
CINECA
ICSC
Centro Nazionale di Ricerca in HPC, Big Data and Quantum Computing
THALES
ECMWF
RI.SE
UNIVERSITÀ
DEGLI STUDI
DI TORINO
SAL
SILICON AUSTRIA LABS

VEC TA: Vector Accelerator

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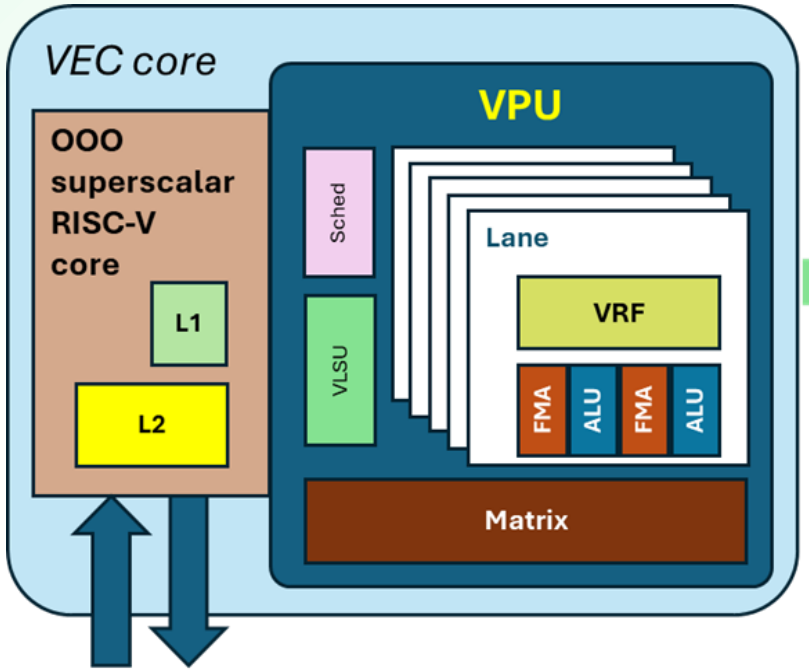
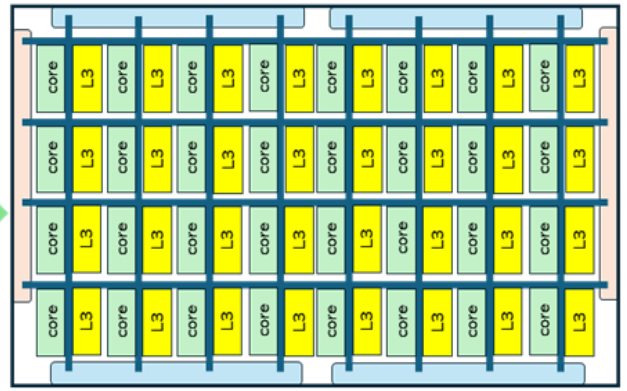
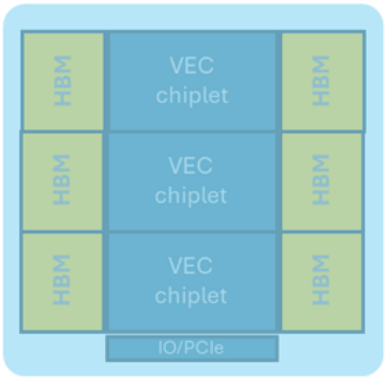
VEC TA objectives

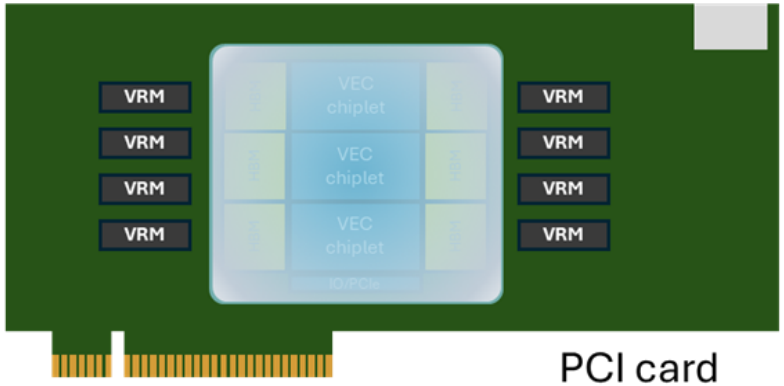




Chiplet
(symbolic representation)



SiP
(symbolic representation)



PCI card
(symbolic representation)

- OOO RISC-V core, RVV-1.0
- Multi-lane long vector VPU
  - VLEN=16kbits
  - Matrix extension for AI
- Many-core chiplet
- Multi chiplet SiP
- HBM memory

INT TA: Integration

Co-funded by the European Union

EuroHPC Joint Undertaking

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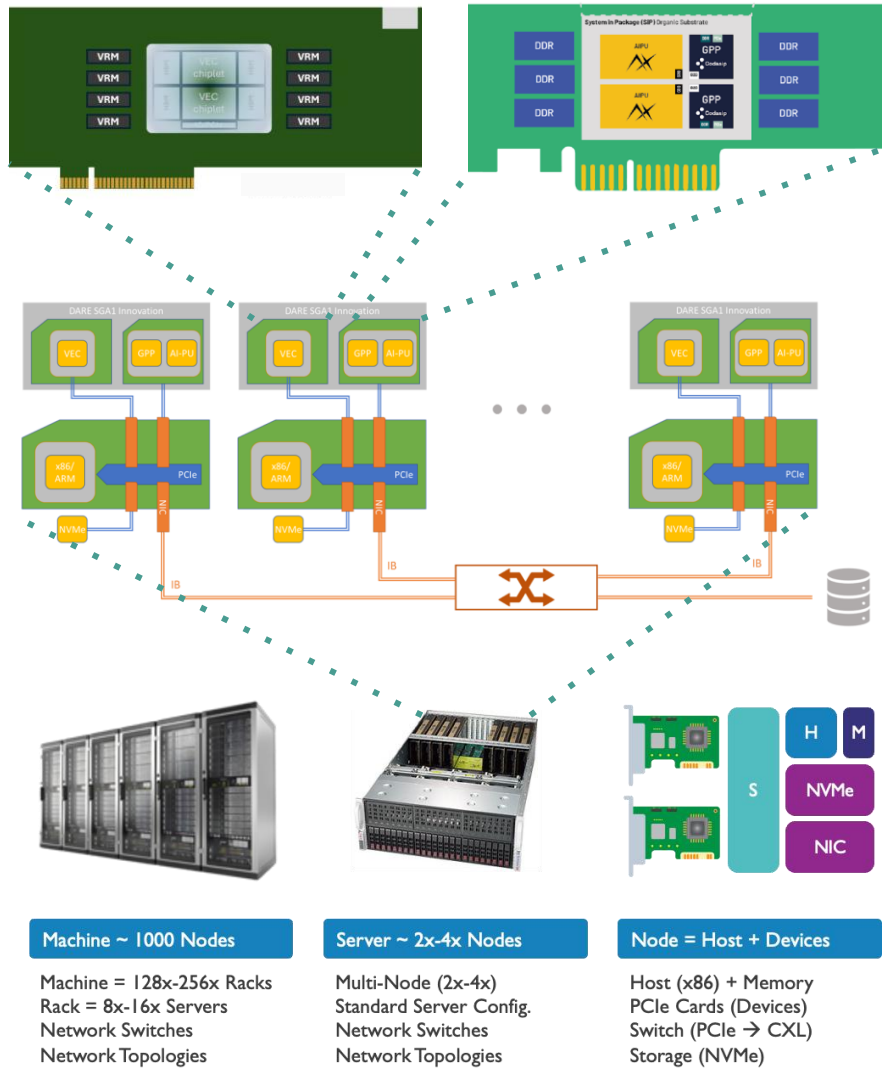
INT TA objectives

- **DARE Devices:** Realisation of a set of DARE devices through physical design of chiplets, design of substrate and silicon interposer and SiPs for chiplet integration, PCB design and fabrication, and bring-up and characterisation of boards
- **Physical Prototype:** Realisation of a multi-node machine with each node housing a standard x86 host and multiple DARE devices (integrated in the form of PCIe cards)
- **Virtual Prototype:** Realisation of a virtual twin of a multi-node (~100×-1000×) machine built as a PDES (parallel discrete event simulator) multi-fidelity model to integrate models of DARE devices at an appropriate abstraction and with the required interfaces (e.g., PCIe, CXL over PCIe/UCIe)

The form factor of the devices, the physical prototype and the virtual prototype in the diagrams are for representative purposes only; to be finalized in the System Architecture Definition phase.



INT TA partners