Pilot using Independent Local & Open Technologies

RISC-V Accelerators: Experiences from the EUPILOT Project

Workshop on Advancing RISC-V Adoption in HPC and Cloud Environments, Bologna, June 12, 2026

The European PILOT project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No.101034126. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Spain, Italy, Switzerland, Germany, France, Greece, Sweden, Croatia and Turkey.

www.eupilot.eu

Overview

Project Information

The European PILOT

Grant agreement ID: 101034126

Funded under

H2020-EU.2.1.1.

H2020-EU.2.1.1.2.

Overall budget

€ 29 999 925

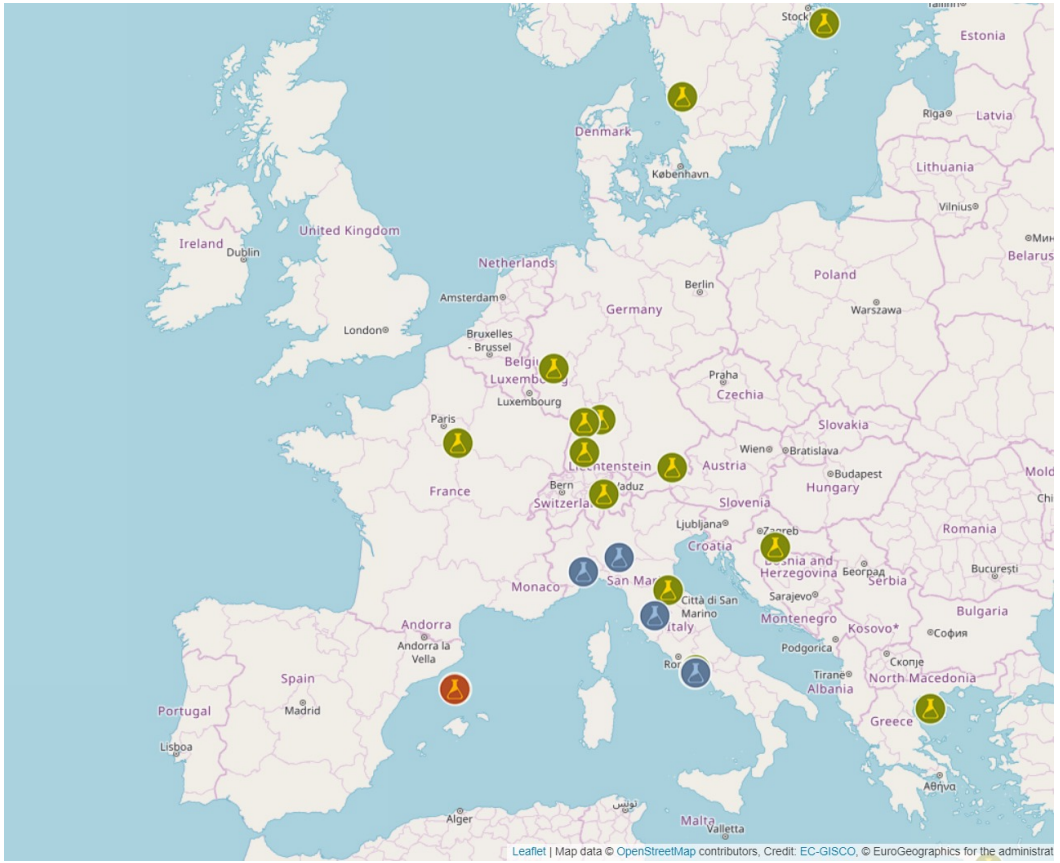
EU contribution

€ 14 999 962,51

Coordinated by

BARCELONA SUPERCOMPUTING CENTER-CENTRO NACIONAL DE SUPERCOMPUTACION

Spain

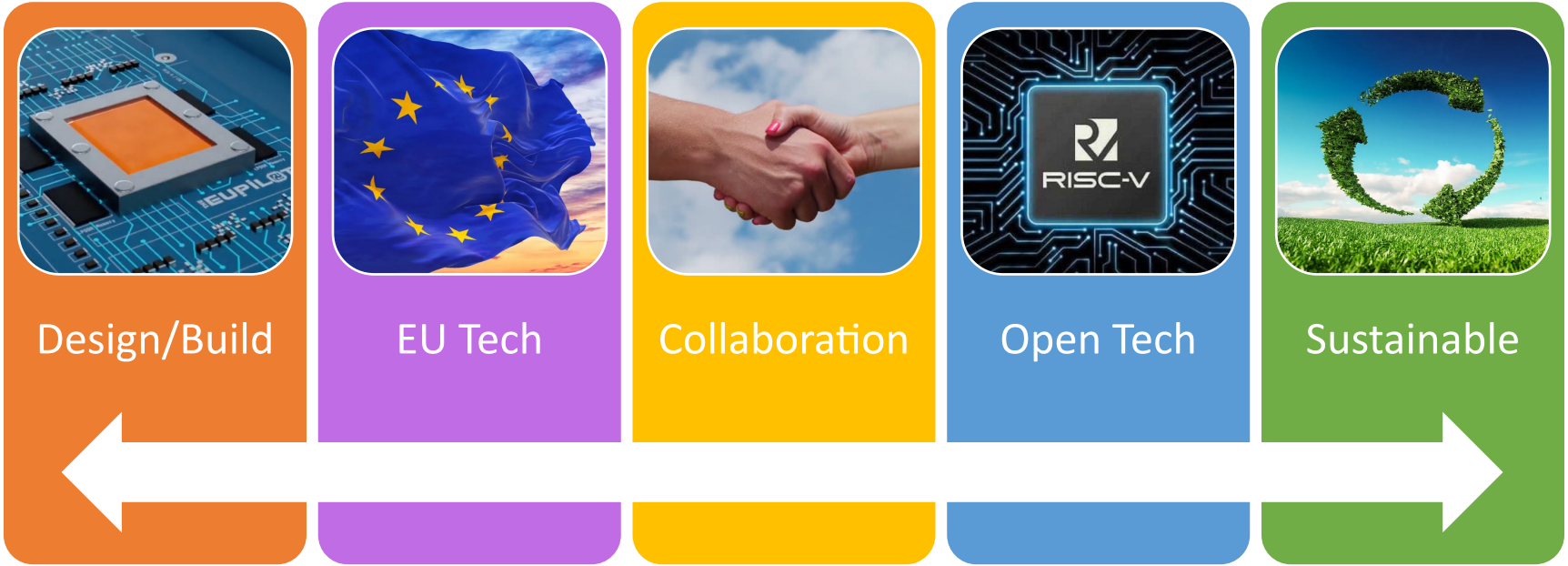


THE EUPILOT

19 Partners

Objectives

➔ **Demonstrate a European pre-exascale accelerator platform**



➔ **Strengthen European Digital Autonomy and HPC & AI supply chain**

User communities (CoEs, …)

Key SW/HW tech

Project: from Chips to Deployment

- **HW: Tape-outs from 22nm → 12nm & 7nm**
  - One test chip
  - Two accelerator chips: **VEC** (GF/12nm) & **MLS** (TSMC/7nm)
- **SW: Target key HPC and AI applications**
  - Port toolchains/libraries/frameworks/apps to RISC-V & RVV
  - Develop toolchains for manual or automatic optimizations
- **Systems: Deploy OCP systems into liquid immersion tanks**
  - Enables higher workloads, density & capacity
  - Reduces environmental impact

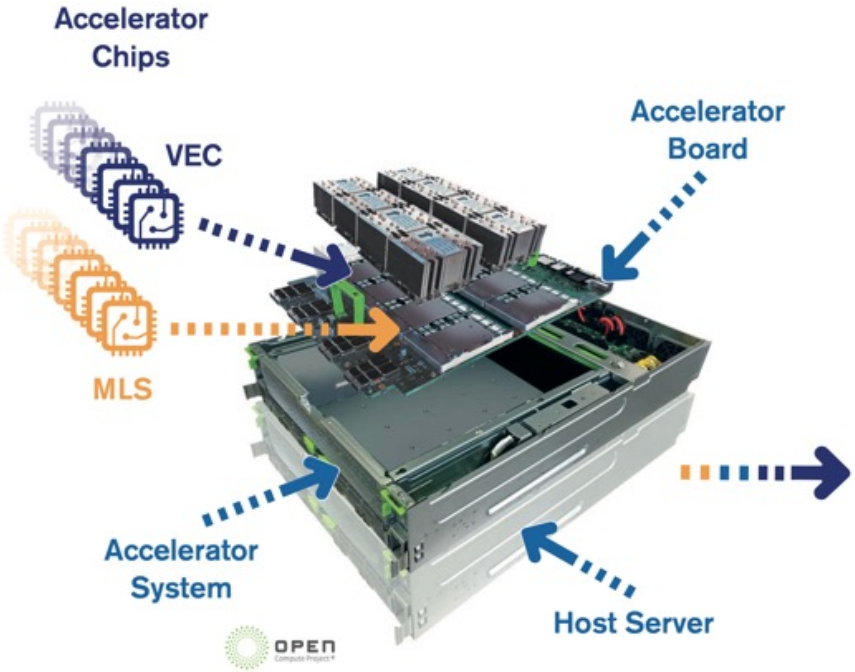
➔ **Deploy EUPILOT *demonstrator* accelerator in a datacenter-like environment**

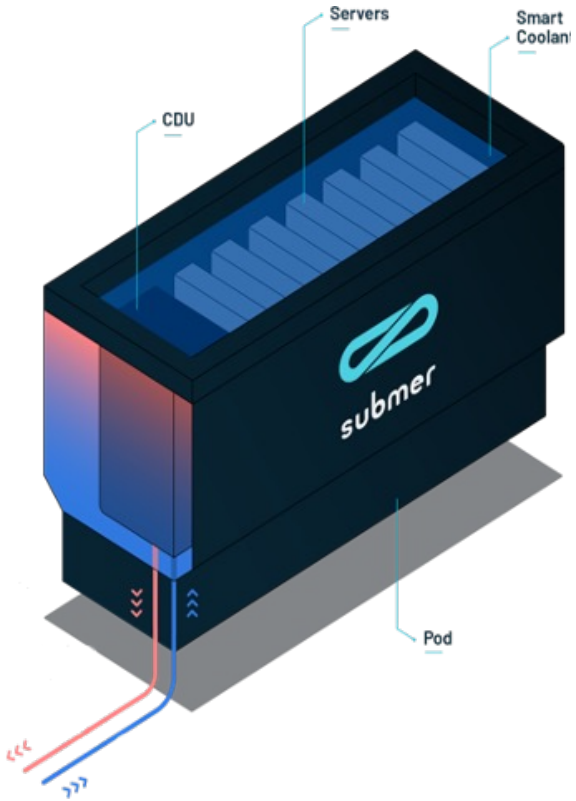
➔ **Ideally become an SDV for later projects**

Target **UBB**

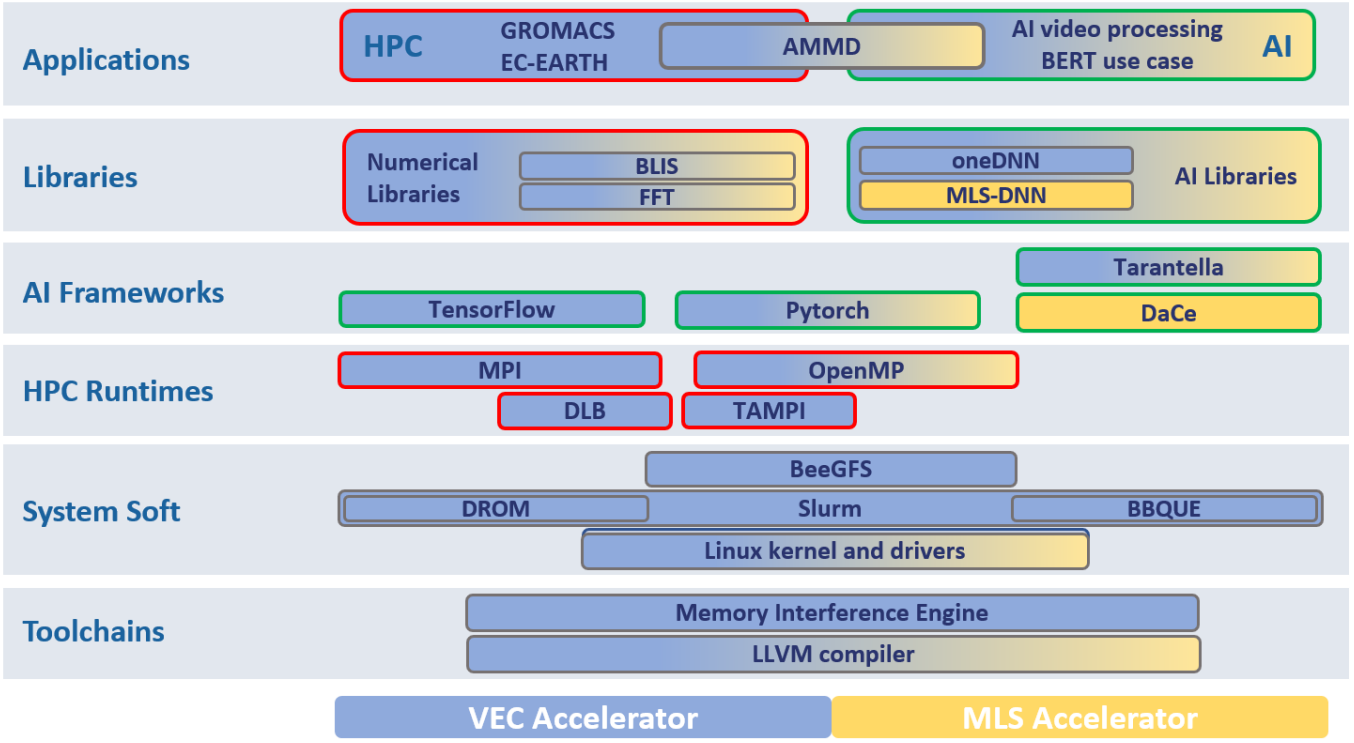
- **By-8 baseboard**
- **Dual quad interconnect**
- **OAM 2.0**

Top Level View

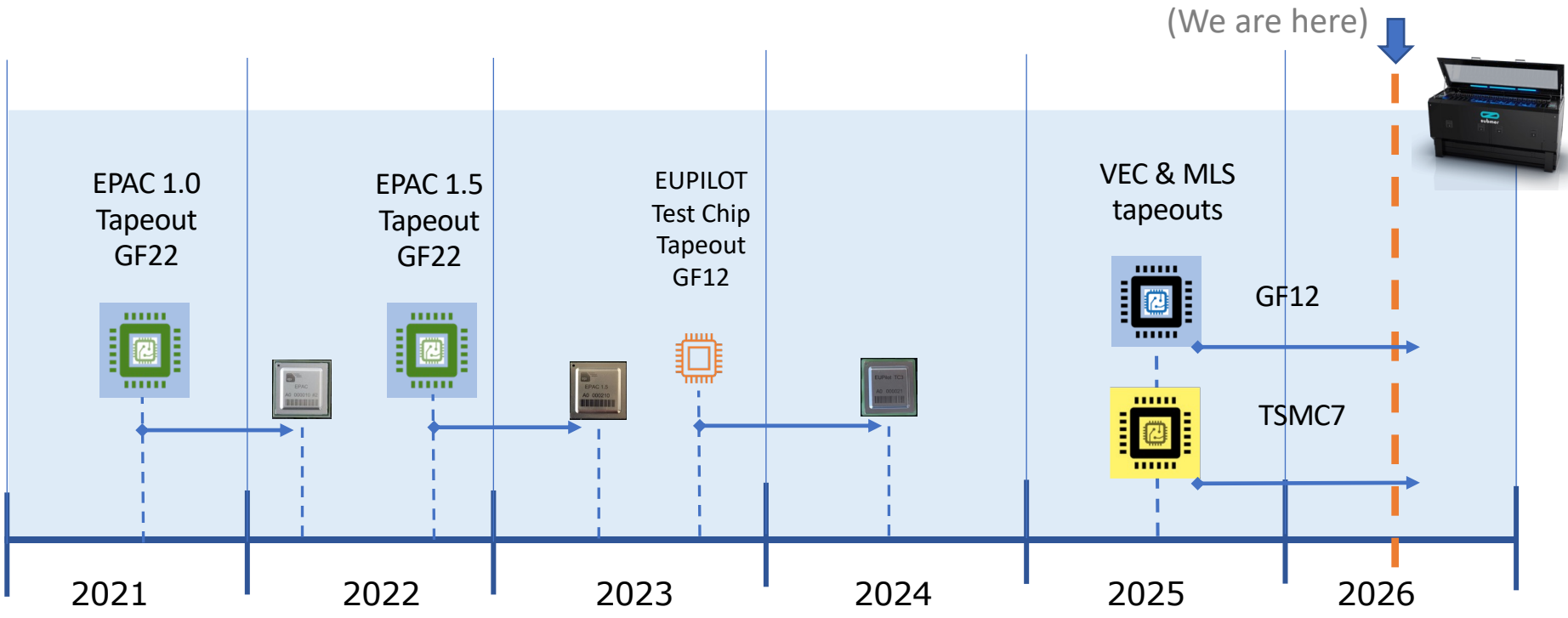




Software Stack



Timeline of Accelerator Tapeouts



VEC
Bare
Die


MPW1440 - RACYICS
Device: MPW1440_BSCVEC
LotID: 8XYC36000
WaferID: PYDOT012MXF2 (#3)
Split: TT
Qty: 16
Gelpack: 1/4
GlobalFoundries
FAB1 Prototype Assembly
MPW1440 - RACYICS
Device: MPW1440_BSCVEC
LotID: 8XYC36000
WaferID: PYDOT012MXF2 (#3)
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Gelpack: 4/4
GlobalFoundries
FAB1 Prototype Assembly
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WaferID: PYDOT011MXB0 (#4)
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Gelpack: 1/4
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Split: TT
Qty: 16
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Split: TT
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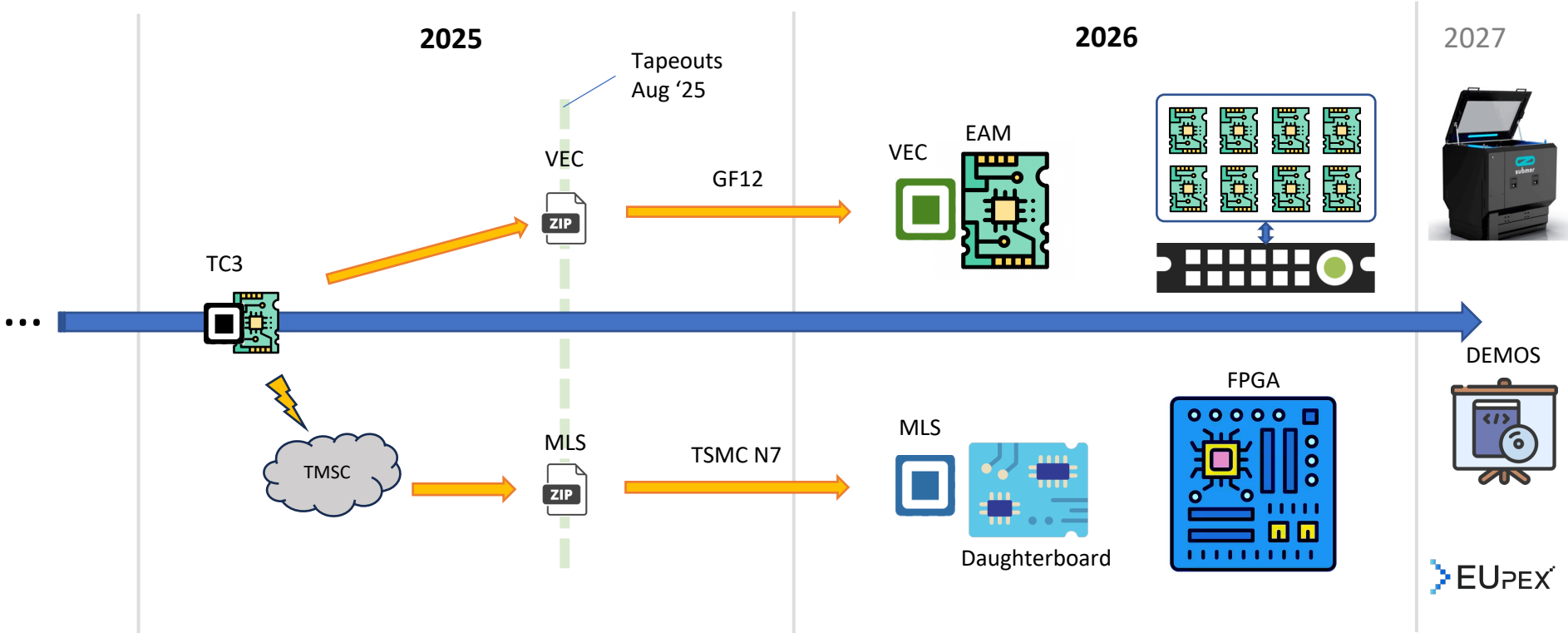
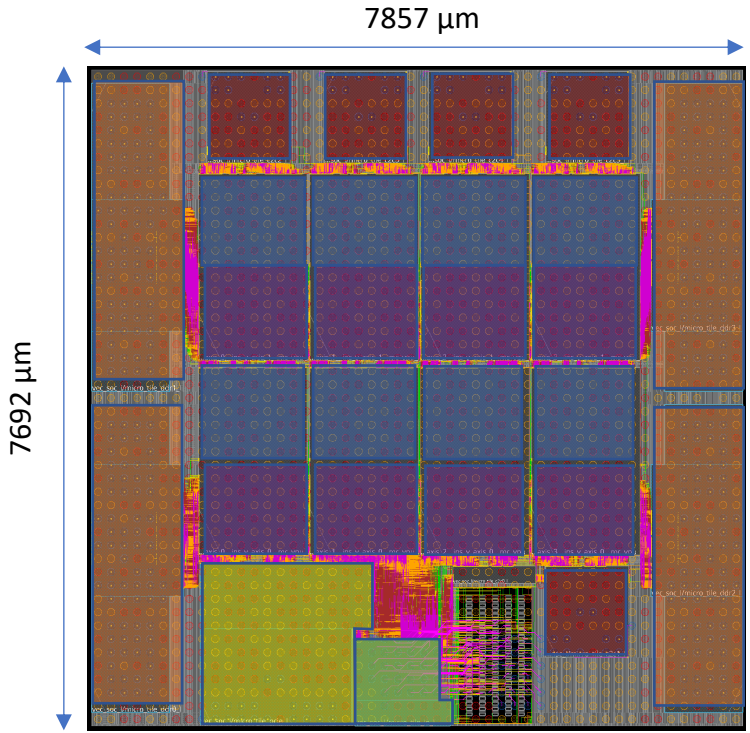
Gelpack: 4/4
GlobalFoundries
FAB1 Prototype Assembly

Recent Timeline

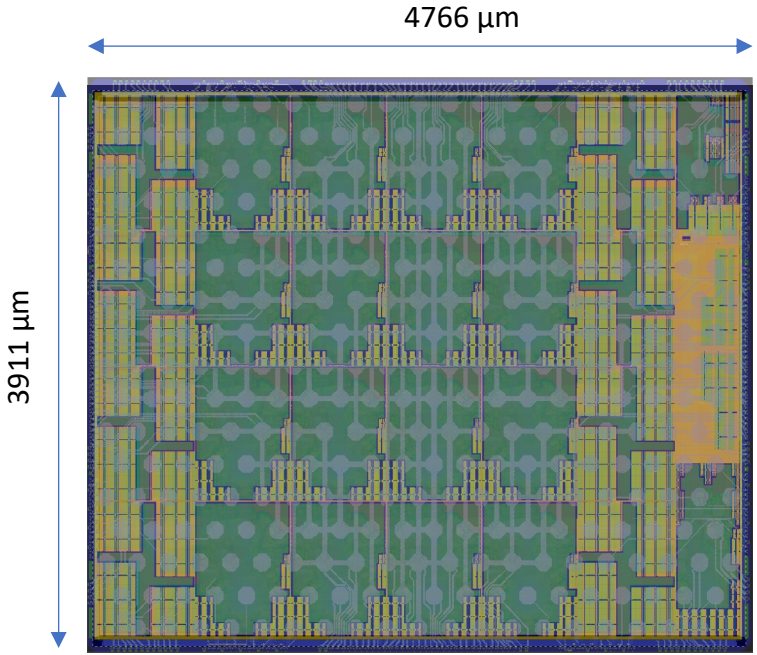


HPC Chip: **VEC** Die



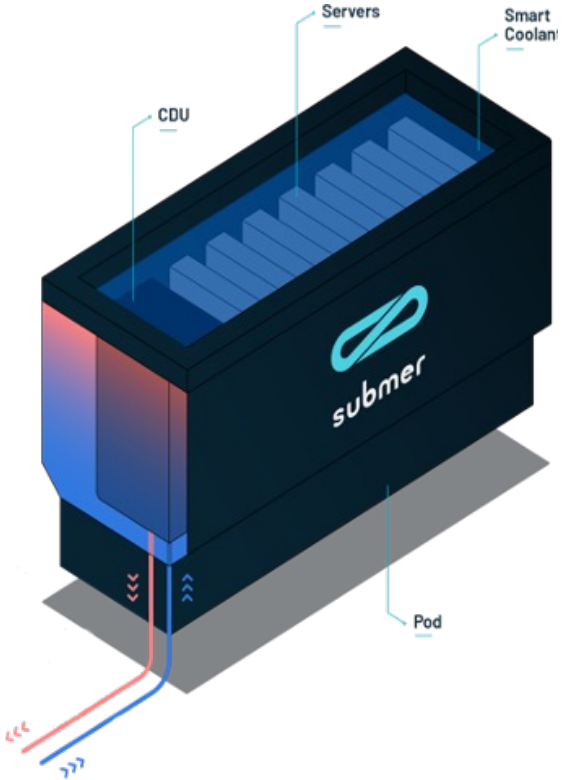
- 8 x 64-bit cache coherent RISC-V cores
- 8 x RISC-V VPUs (Vector Processing Units)
- 4 x LPDDR4 @ 2.133GHz (w/RISC-V PHY)
- 5 x C2C links @ 32Gbps
- 1 x CXL2/PCIe5 @ 32Gpbs
- 1 x 32-bit RISC-V chip (I/O controller)
- Target @ ~1GHz

AI Chip: **MLS** Die



- 16 x Clusters
- 9 x RISC-V cores/cluster
- 10 MB on-chip memory
- STX cluster (Fraunhofer)
- Target @ 1 GHz

Ultimate Targets: Demonstrations



Experiences in EUPILOT

- **Goal wise**
  - Mighty ambitious goals ☣️
  - Not realistic for the timeline & team ⚠️
  - Periodically shrunk/adjusted when reality set in ✅
  - Were able to take advantage of opportunities
- **Project wise**
  - Limited budget vs. goals ⚠️
  - Hampered by 50/50 rule of national funding ☣️
  - Constrained by many & very slow administrative rules
  - Open-source and RISC-V helped ✅ .. however, industry is not mature ⚠️
  - Obtaining proprietary licenses/libraries/tools took forever ⚠️
  - Verification/integration efforts well below industry standards ☣️
  - Slippages happened, causing ripple effects ☣️
- **Organization wise**
  - Too many partners
  - Teams smaller than pie-in-the-sky goals ⚠️
  - Disparate groups/teams with limited overlap
  - Participants overcommitted in many projects ☣️
  - Partner types led to conflicting goals: research vs. industry ⚠️

Thank You

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