The CAPE project has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement No 101189899.

CAPE

European Open **C**ompute **A**rchitecture for **P**owerful **E**dge

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Composable Heterogeneous Edge Infrastructure in CAPE

From Edge AI to RISC-V Acceleration

Christian Klarhorst, Bielefeld University

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Agenda

- Overview & Vision
- Composable Hardware Platforms
- Open Software Architecture
- Edge-Cloud Use Cases
- RISC-V Integration and Acceleration

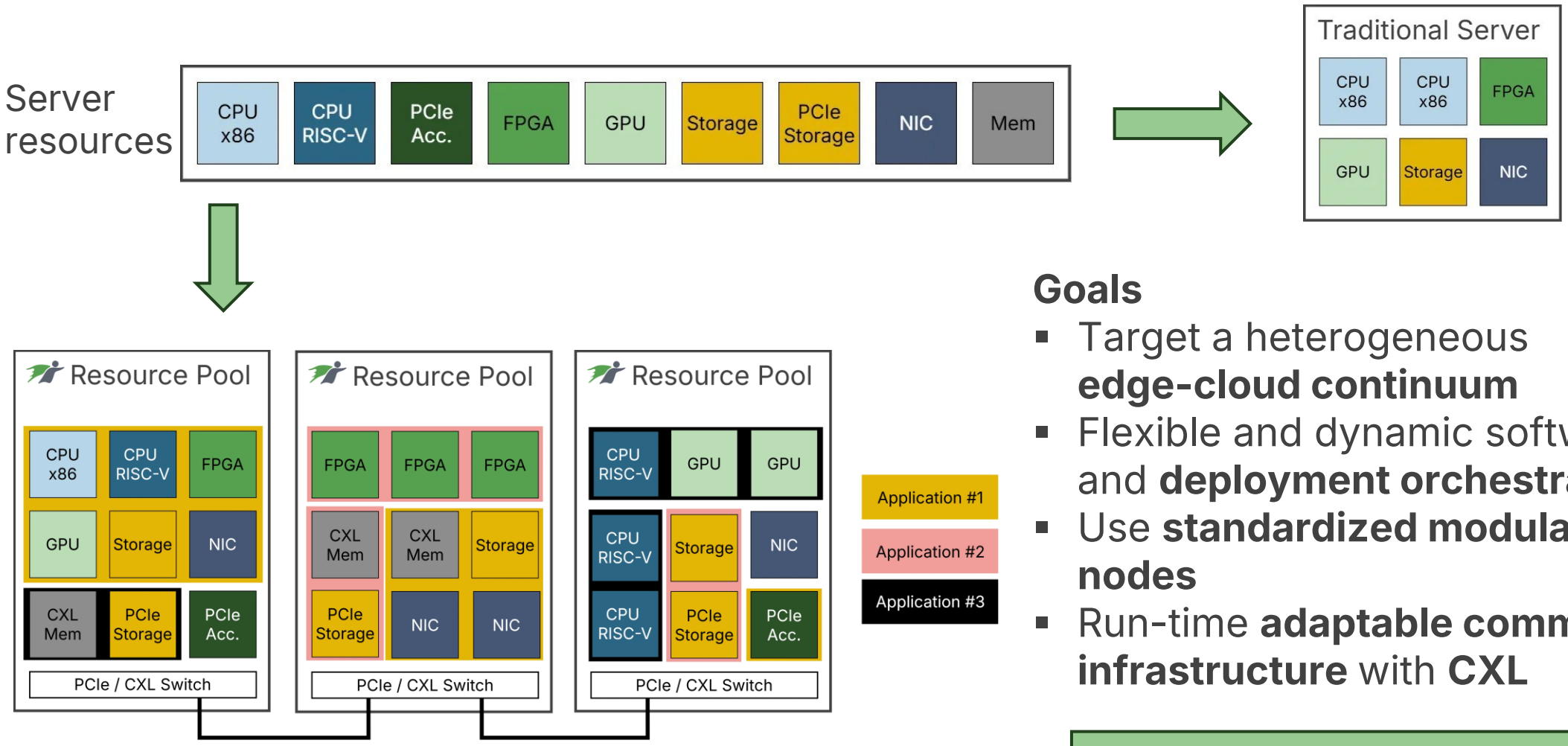
CAPE - European Open Compute Architecture for Powerful Edge

Related HU project in the same call:

- EU-Call: „Open Source for Cloud/Edge to support European Digital Autonomy" (Horizon CL4 2024 Digital Emerging 01-21)
- Start: 12/2024
- Consortium
  - 7x Industry (6x SME)
  - 4x Academic
  - 1x Standardization organization
- Coordinator: Bielefeld University

* associated participants

CAPE's Vision
Towards a Composable Server Infrastructure



Resource Pools → Composable Infrastructure

Goals

- Target a heterogeneous **edge-cloud continuum**
- Flexible and dynamic software stack and **deployment orchestration**
- Use **standardized modular compute nodes**
- Run-time **adaptable communication infrastructure** with **CXL**

CXL (Compute Express Link) is based on the PCIe transport layer and provides for cache-coherency and memory pooling

Big Picture of CAPE

Use Cases

Smart Grid

Edge AI

Satellite Payload Processing

Standardization

OFEIA

(**O**pen **F**ederated **E**dge-Cloud **I**nfrastructure **A**lliance)

COM HPC

Open Edge Server Management

- Web-based, out-of-band configuration
- Run-time topology reconfiguration
- Live power monitoring
- Support for heterogeneous computing nodes

Edge cluster → Edge servers → Compute nodes

Software Services

- **I**nfrastructure **f**rom **C**ode (IfC)
- AI-assisted orchestration and service deployment
- Resource clustering: dynamic node allocation & composition

Edge-Cloud Continuum

IoT · Telco · Industry 5.0 · Automotive · AI / ML · HPC

Hardware

Modular, Heterogeneous Compute Nodes

x86 · FPGA · RISC-V @FPGA · GPU SoC · RISC-V · CXL memory

Supported Edge Server

eHPS … (up to 3 nodes)
embedded **H**igh-**P**erformance **S**erver

EMDC ……. (up to 7 nodes)
Edge **M**icro **D**ata **C**enter

Third party .. ||||| on-premises or cloud

Environment Integration

- Wall mount & 19" rack
- Hybrid: passive and active cooling
- Waste heat recovery

Big Picture of CAPE

Use Cases

ipto

Smart Grid

Edge AI

PCB DESIGN

Satellite Payload Processing

Fraunhofer ITWM

Standardization

UNIVERSITÄT BIELEFELD

OFEIA

(**O**pen **F**ederated **E**dge-Cloud **I**nfrastructure **A**lliance)

COM HPC

Open Edge Server Management

PICMG

- Web-based, out-of-band configuration
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CHRISTMANN INFORMATIONSTECHNIK + MEDIEN

Edge cluster → Edge servers → Compute nodes

Software Services

Universität St.Gallen

- **I**nfrastructure **f**rom **C**ode (IfC)
- AI-assisted orchestration and service deployment
- Resource clustering: dynamic node allocation & composition

hiro Edge Micro Data Centers

ryax technologies

Edge-Cloud Continuum

IoT · Telco · Industry 5.0 · Automotive · AI / ML · HPC

Modular, Heterogeneous Compute Nodes

Hardware

x86 · FPGA · RISC-V @FPGA · GPU SoC · RISC-V · CXL memory

parallel efficiency matters

PCB DESIGN

Fraunhofer ITWM

Supported Edge Server

UNIVERSITÄT BIELEFELD

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PCB DESIGN

Wall mount & 19" rack
Hybrid: passive and active cooling
- Waste heat recovery

Environment Integration

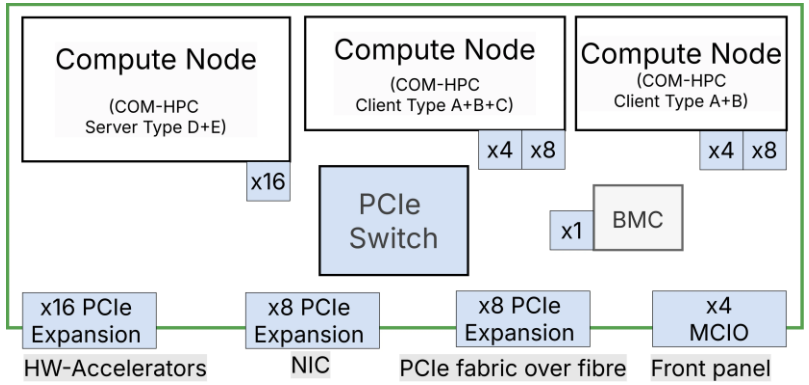
Cadterv

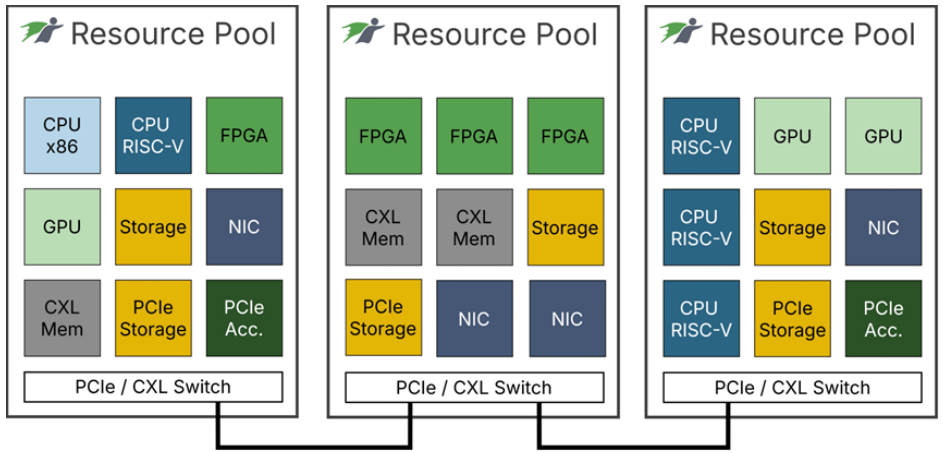
EPFL

Hardware Platforms

UNIVERSITÄT BIELEFELD · CHRISTMANN INFORMATIONSTECHNIK + MEDIEN · paraXent efficiency matters

eHPS: embedded **H**igh **P**erformance **S**erver



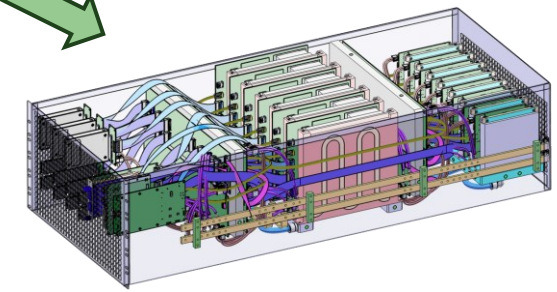


Heterogeneous edge servers

Two implementations

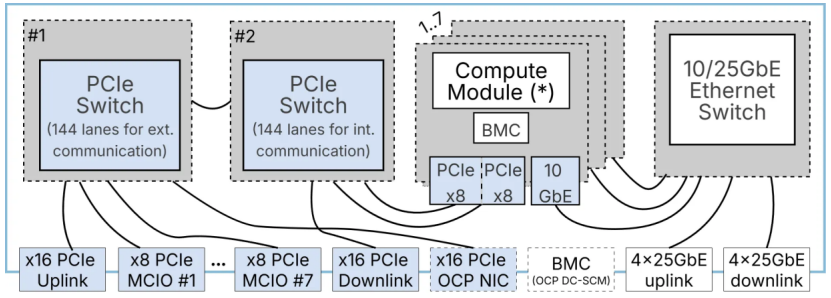
Hybrid cooling & building integration

CAPE's fully Composable Infrastructure



PCB DESIGN

EMDC: Edge **M**icro **D**ata **C**enter



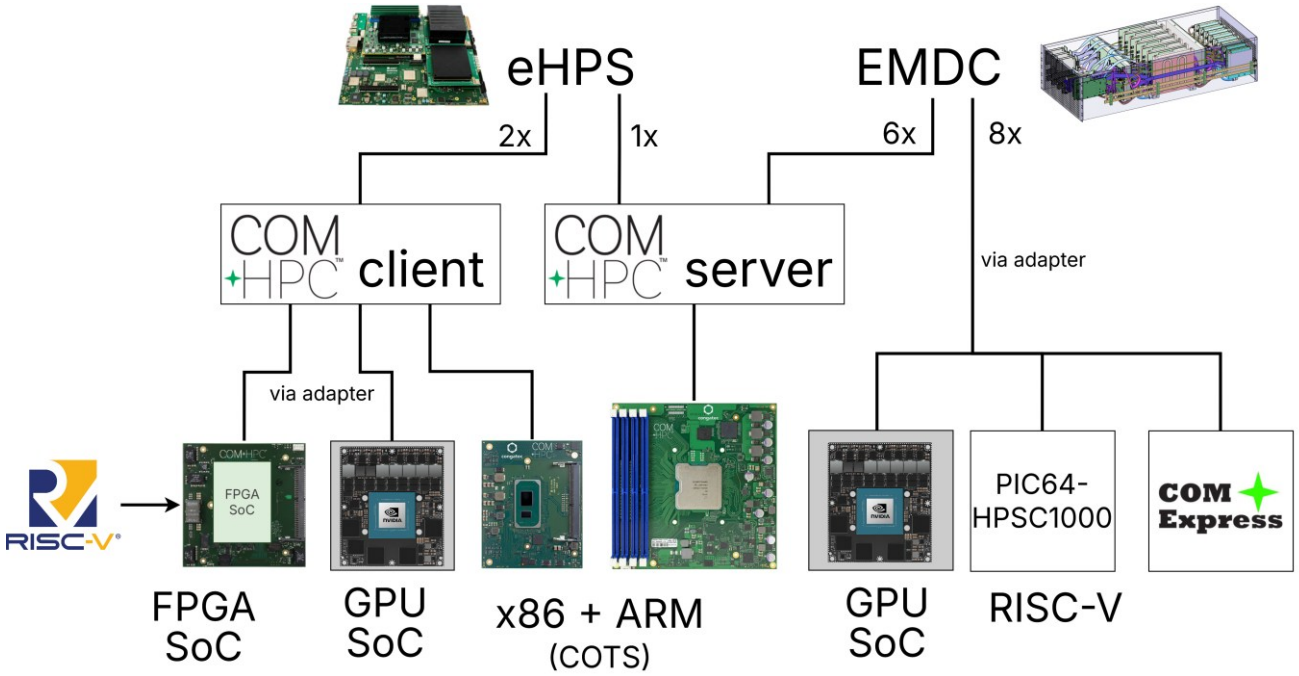
(*) Supported compute modules: COM-HPC Server Type E, Jetson AGX

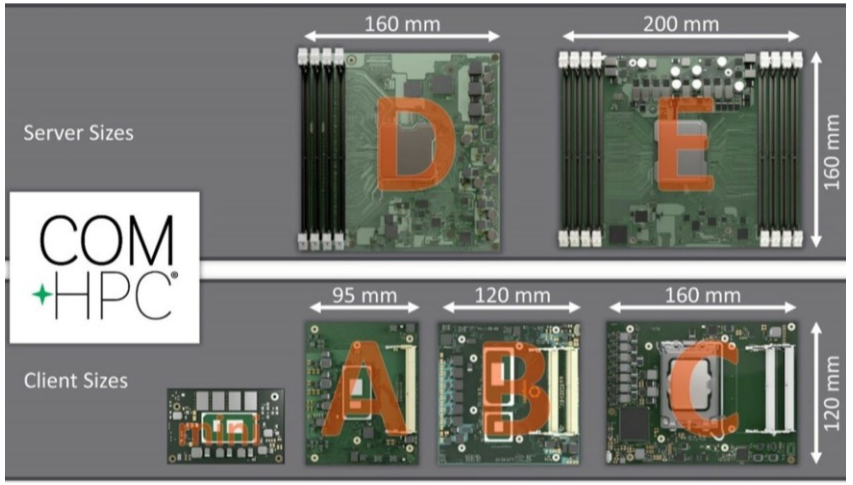
----- exchangeable module ~~~ interconnect by cable

EPFL Cadterr

CAPE's Hardware Platforms

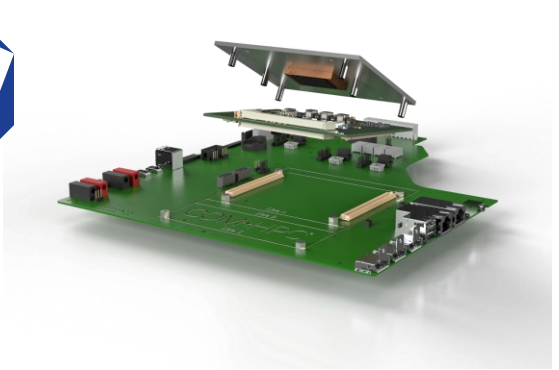
- Two carrier boards: eHPS and EMDC
- Based on well-established COM (Computer-On-Module) form factors
- Focus on heterogeneous computing





COM-HPC Module Overview

PICMG®



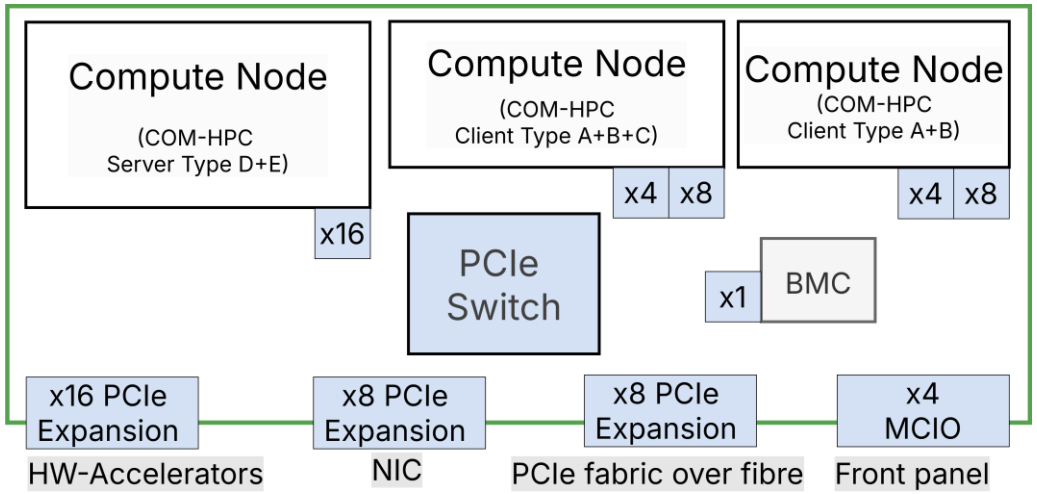
COM-HPC is a computer-on-module form factor standard for high performance edge applications

eHPS – embedded High Performance Server

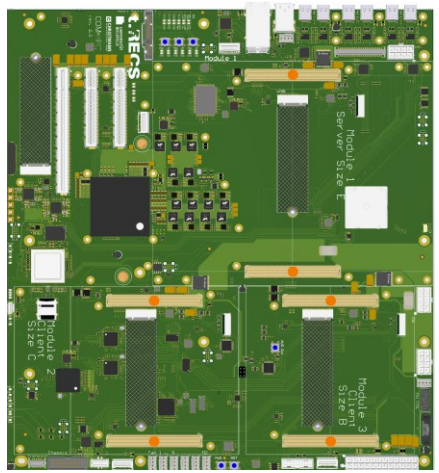
3 height units 19“ server

- 3x COM-HPC compute modules
- PCIe Gen6 /CXL -based communication infrastructure
- Power budget 500W-5000W
- Widely available air-cooled 19” rack server housings (E-ATX form factor)

eHPS predecessor „t.RECS“ using PCIe Gen3



eHPS PCIe-centric architecture



Rendering of eHPS PCB

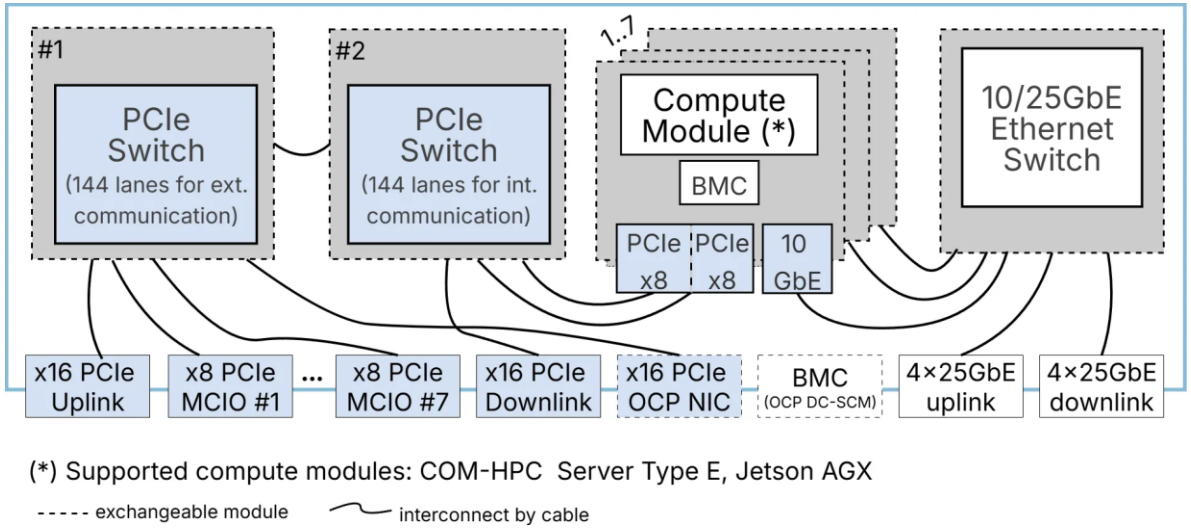
PCIe/CXL Fabric: PCIe Gen6 First, CXL Ready

PCIe Gen6 today

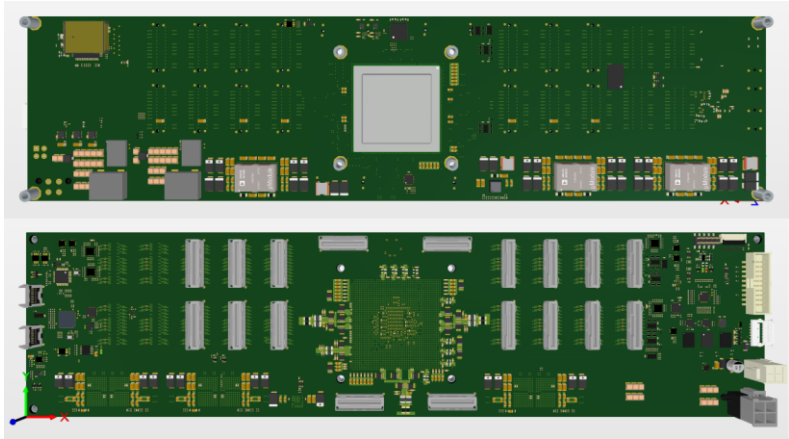
- 64 GT/s per lane, PAM-4, FEC, FLIT framing
- High-speed module interconnect
- Host-to-host communication
- Accelerator, storage and NIC sharing

CXL roadmap

- Based on PCIe physical layer
- CXL.io, CXL.cache, CXL.mem
- Memory expansion and pooling
- Coherent accelerator and memory access



Block Diagram of the PCIe/CXL switching fabric



Rendering of PCIe/CXL switch PCB

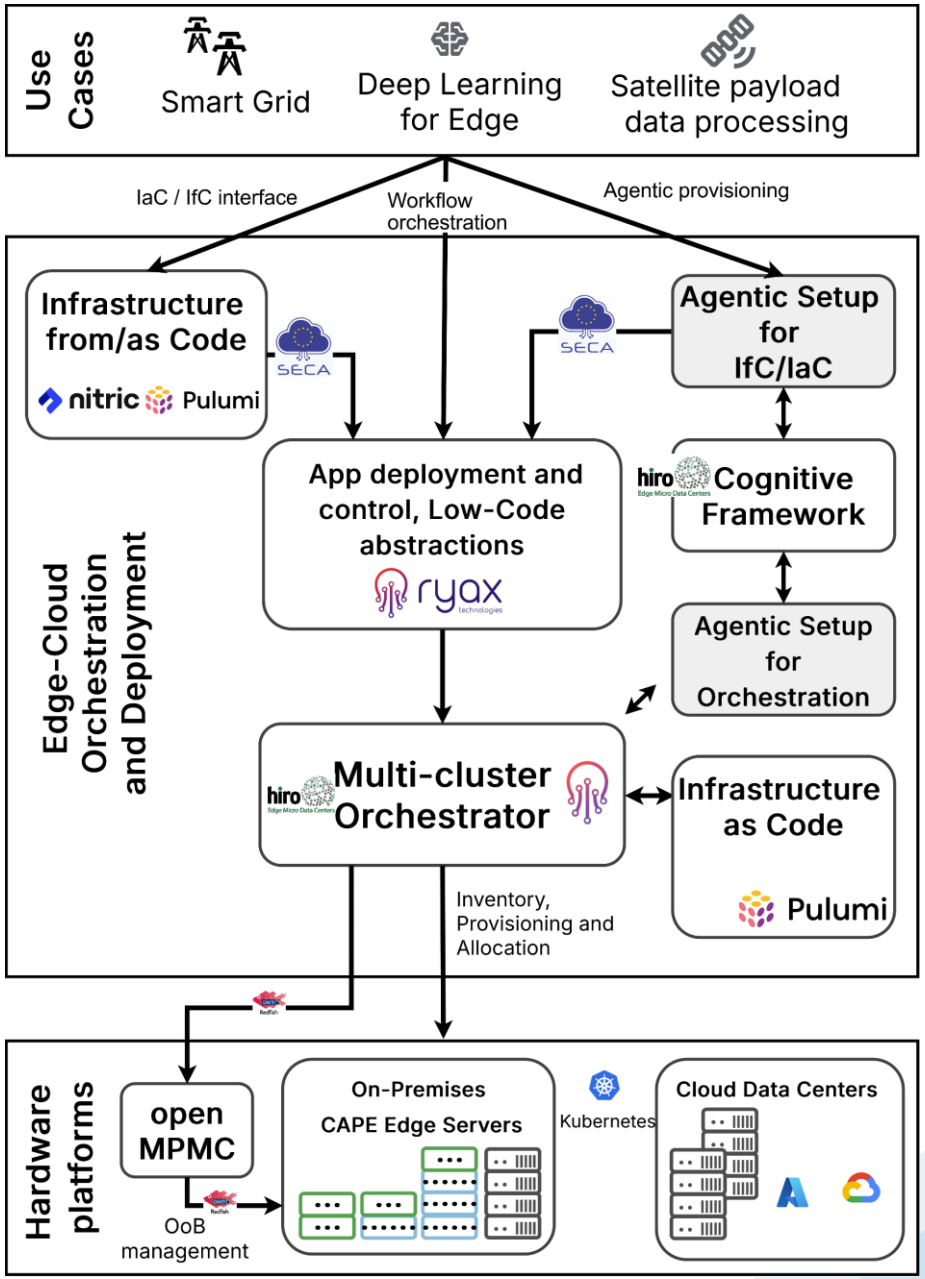
Software Architecture

Features

- Transparent deployment across edge-cloud continuum
- Heterogeneous computing resources
- Three different programming and deployment models
- Fully open source stack including (Sovereign European Cloud API)

Components / tools

- Infrastructure from/as Code (IfC/IaC): Automated Software Testing
- Ryax: Deployment, resource selection and data center management
- Orchestrator: manages inventory, configures network infrastructure and compute nodes
- openMPMC (Multi-Platform Management Controller): low-level server management

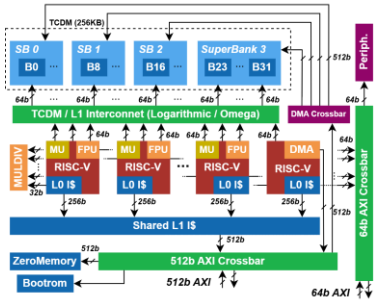


Use Case Overview

Edge AI

- Surveillance on RISC-V / FPGA with accelerators
- Optimize deep learning algorithms
- **Low-latency & high throughput**

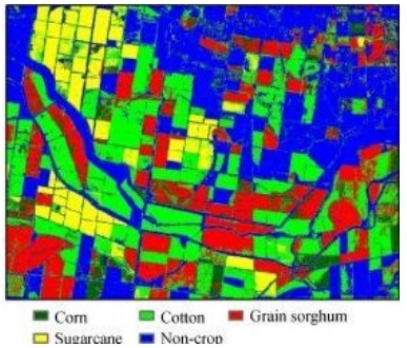
Fraunhofer ITWM



Satellite Payload Processing

- Data-(pre-)processing
- Data clustering & fusion
- **High throughput & energy efficiency**

PCB DESIGN



Smart Grid

- Real-time anomaly detection
- Energy forecasting & market prediction
- **Robustness & real-time capabilities**

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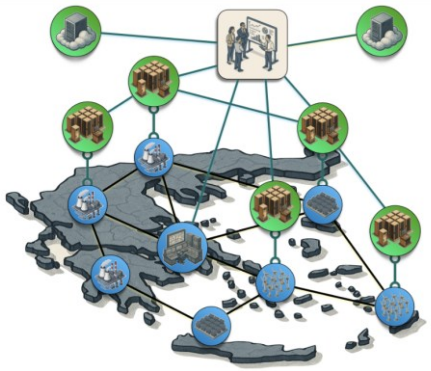


Two RISC-V Paths in CAPE

RISC-V CPU module

PCB DESIGN

- Microchip PIC64-HPSC high-reliability RISC-V processor
- 8× 64-bit SiFive X280 application cores with vector extensions
- PCIe Gen3 x8 + CXL 2.0 (proprietary)
- Secure boot, lockstep, ECC and tamper resistance

RISC-V on FPGA

Fraunhofer ITWM

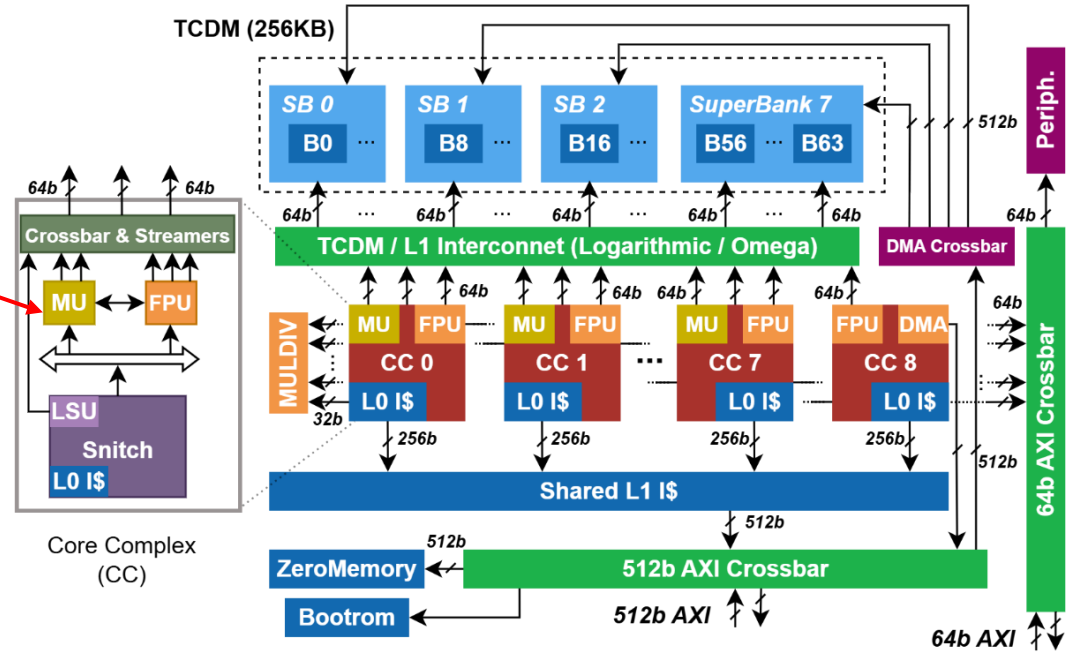
- Snitch-based RISC-V compute cluster
- Snitch + Matrix Unit coupling from EPI pilot study
- FPGA-based exploration of RISC-V DL acceleration
- Matrix Unit exploration for matrix-dominated DL kernels

FPGA SoC (COM-HPC)

RISC-V DL Accelerator on FPGA

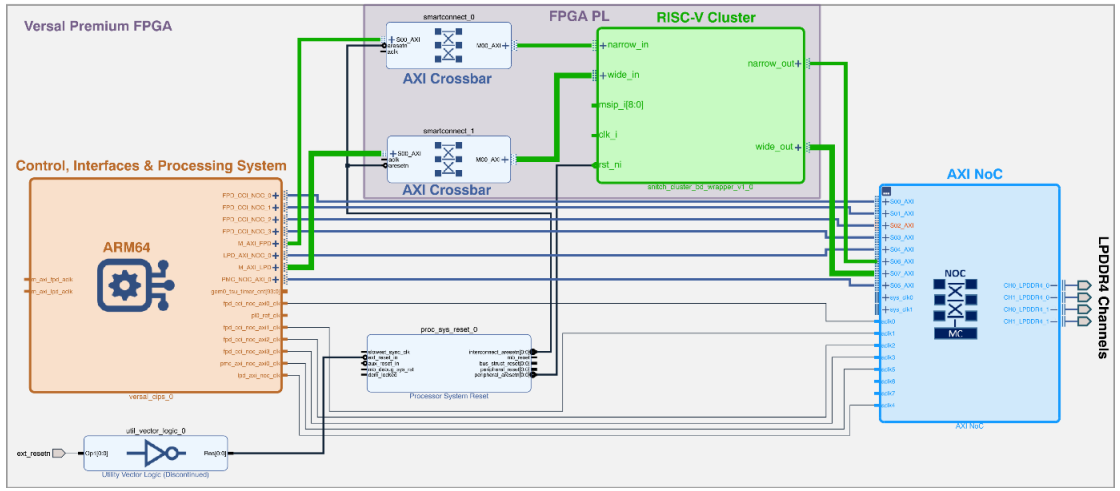
- 8 worker Core + 1 DMA Core Complexes
- RV32I Snitch control cores
- FP32/BF16 FPU + Matrix Unit
- 256 KB shared TCDM scratchpad
- Streaming support for regular memory access
- 512-bit AXI DMA path
- Burst and 2D transfer support
- CAPE: FPGA integration and verification
- CAPE: DL kernel evaluation / benchmarking

Matrix Unit (MU)



From FPGA Prototype to CAPE Integration

- AMD VPK120 with Versal Premium FPGA
- PCIe Gen5 platform with CXL 2.0 soft-IP option
- ARM host runs lightweight Linux
- RISC-V cluster instantiated in FPGA fabric
- 2 GB DRAM reserved for cluster execution
- Bare-metal tests executed successfully



Next Steps:

- Versal Premium Gen2 with PCIe Gen 6 and CXL 3.0
- Prepare CXL integration and configuration
- Explore CXL-based coherent accelerator and memory access

RISC-V in CAPE: Key Takeaways

- CAPE integrates RISC-V into heterogeneous edge infrastructure
- Two paths: reliable CPU modules and FPGA-based acceleration
- Satellite payload processing benefits from high-reliability RISC-V
- Edge AI drives adaptable RISC-V acceleration
- PCIe/CXL connects compute, accelerators, storage and memory
- Open software turns hardware into deployable resources

Open processor architectures become more useful when they are integrated into composable, managed and deployable edge systems.

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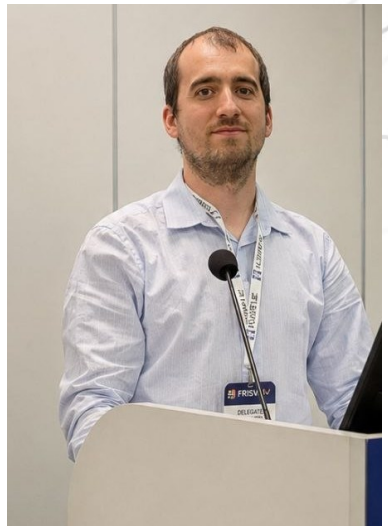

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