Towards European RISC-V Systems: Integration Experiences from the RISER Project

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RISC-V Summit Europe 2026 - Workshop on “Advancing RISC-V Adoption in HPC and Cloud Environments”

European Commission
Horizon Europe 2021-2027

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Project Mission Statement

Can we design and build data-center system platforms based on open standards in Europe today?

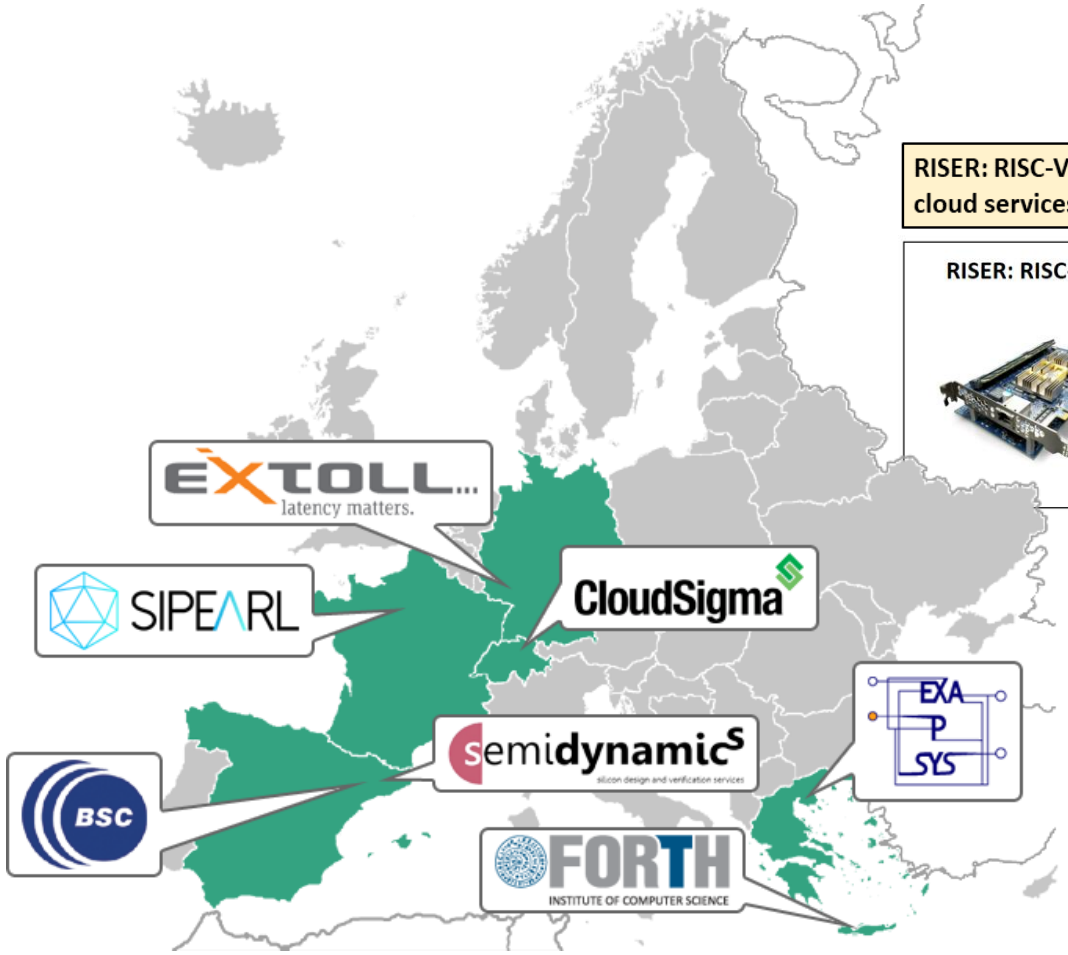
Open standards for ISA == RISC-V

+ Arm ISA (sovereignty-focused projects funded by EuroHPC Joint Undertaking, mainly for HPC)

+ Cloud infrastructure roadmap

RISER in a nutshell

https://zenodo.org/communities/riser/records



RISER: RISC-V based Linux server for cloud services, built on open interfaces

RISER: RISC-V for Cloud Services

RISC-V Processors
Source: EPI and EUPilot projects (chips)
* Currently operating on system boards designed for dev/test purposes

Server Boards (PCB + firmware)
Standard form factors (PCIe accelerator card, Microserver)
* Following industry standards to utilize server I/O peripherals

- DRAM Memory
- NVM-Express Storage
- 100 Gbps Ethernet

Boot Firmware
Initialization of execution platform, Including high-speed I/O peripherals (storage, networking)

OS, drivers, runtime
Configured/adapted for cloud services: workload acceleration, networked storage, containerized execution
*Integration in IaaS environment

https://riser-project.eu

https://www.linkedin.com/company/riser-project/

https://twitter.com/RiserProject

Integrated all-European Hardware and Open-Source Software for Cloud Services and Applications

[RIA Project started on Jan. 1, 2023]

Results

- **Chips from the EPI project → basis of platform prototypes**
  - **Host-Accelerator**
    - **Host: Arm HPC SoC, by SiPEARL**
    - **Accelerator: RISC-V SoC, with the Avispado core by Semidynamics**
  - **Microserver**
    - **Standalone (FPGA-assisted), using RISC-V SoC**
    - **upcoming: variant based RISC-V SoC from the EUPILOT project**
- **Open-source designs, incl. Firmware, OS, runtimes**
- **Use cases:**
  - **Acceleration: OpenMP multi-device task offload**
  - **Cloud: Containers & Orchestration (Kubernetes) runtime, IaaS, Networked Storage**

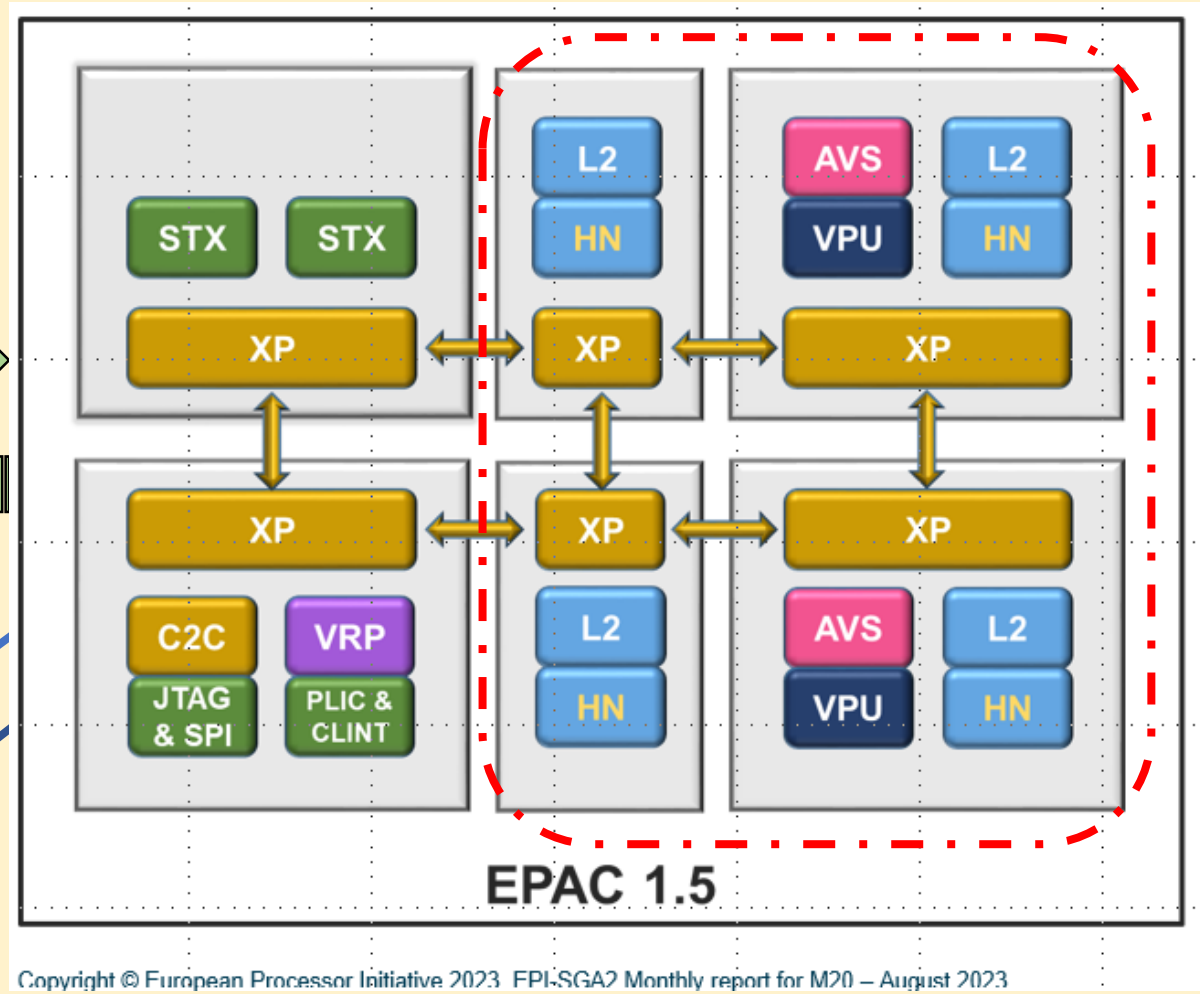
EPAC1.5 (from EPI-SGA2)

EPAC1.5 test-chip from EPI.
- No on-chip Memory & PCIe controllers
- Requires external Config/Boot

Development Host:
- JTAG (for reset/control)
- PCIe controller for loading FPGA memories with boot images

EXTOLL NoC Cross-Points & Chip-to-Chip links

FPGA Board (Memory Controller, PCIe endpoint)

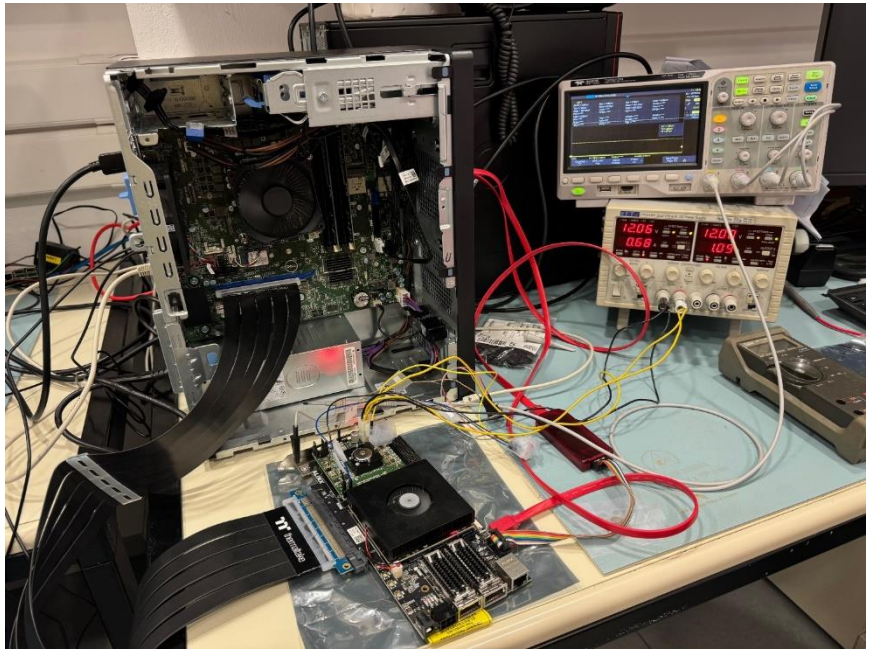


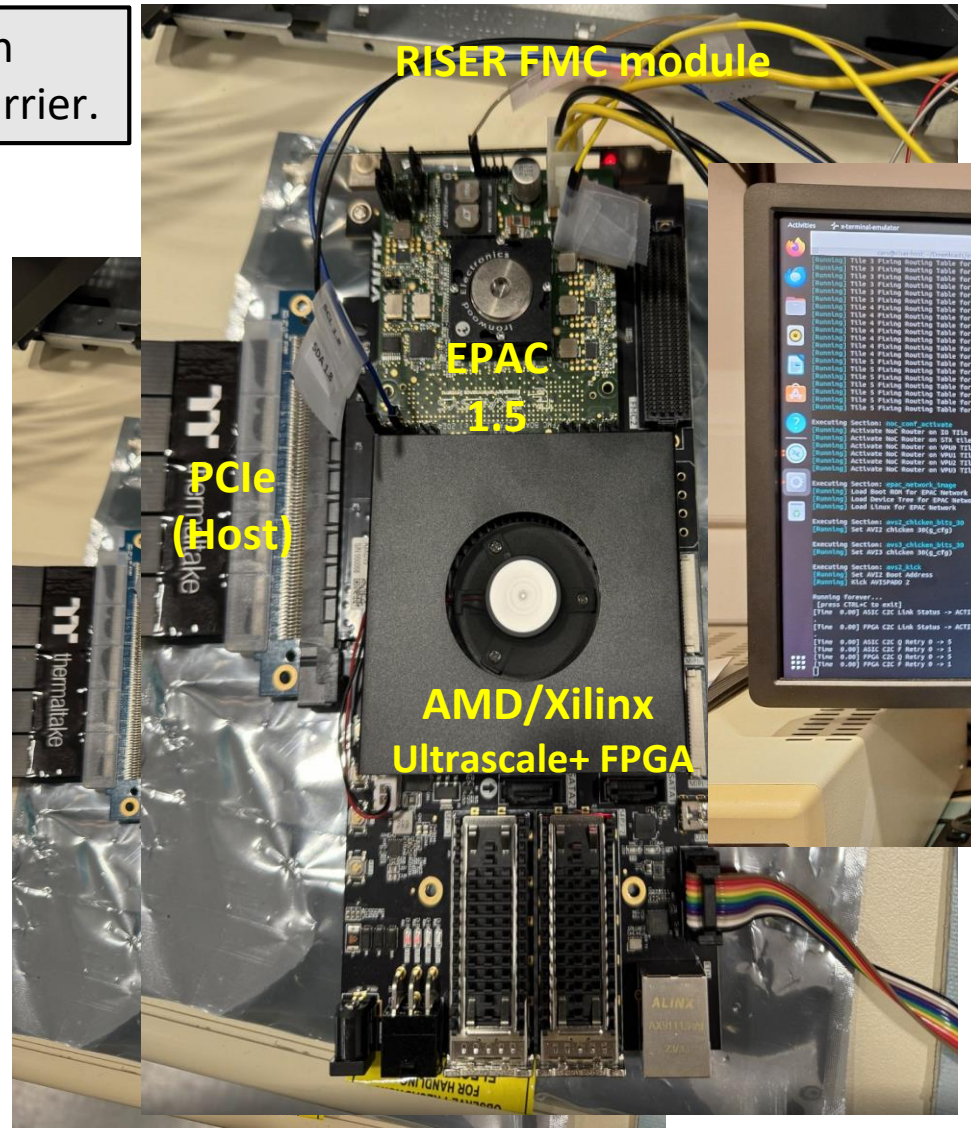
SMD RISC-V + BSC vector + FORTH L2 cache

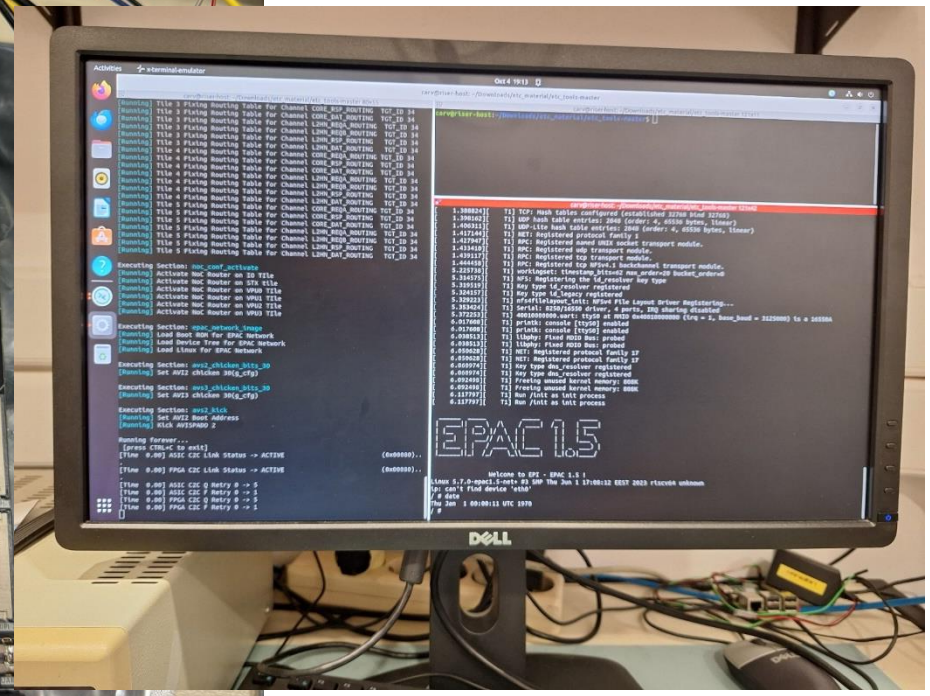
FPGA (FMC+) Daughterboard

Prototypes using test-chip from EPI

PCIe-hosted Accelerator: test-chip hosted on miniaturized FMC daughtercard on FPGA carrier.





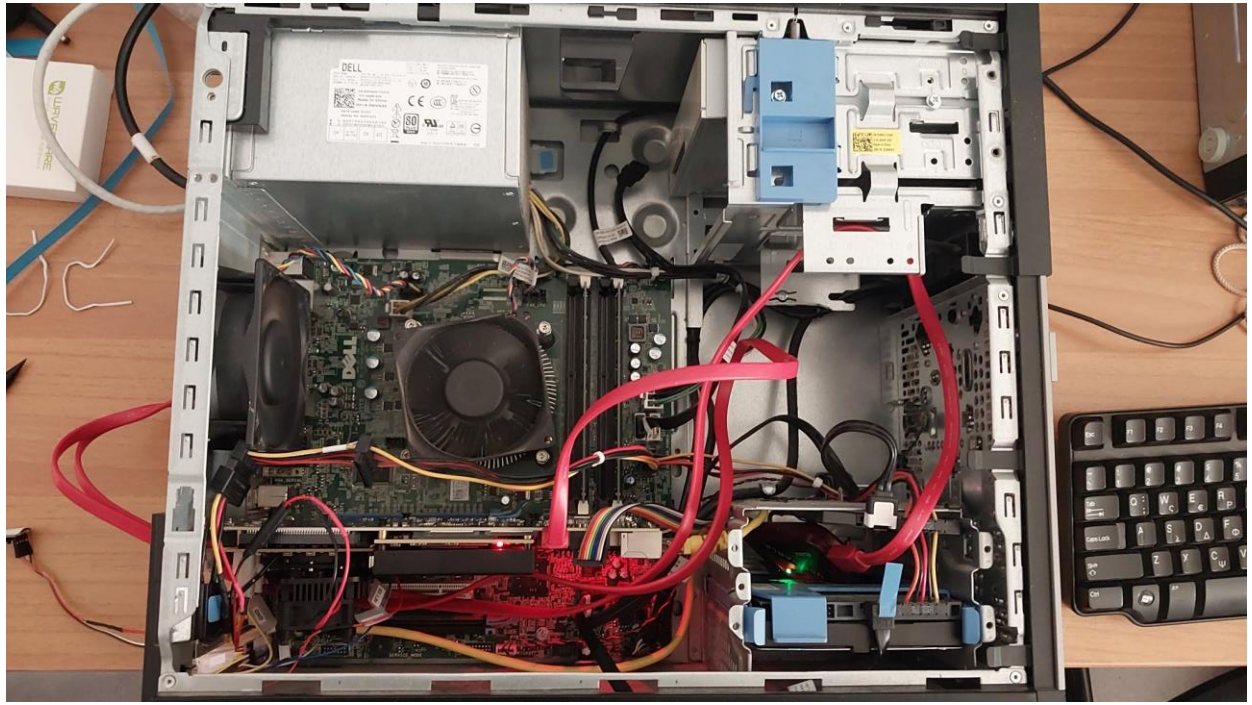


Ongoing effort:
(i) Host+Accelerator (task offload)
(ii) Microserver (self-hosted, I/O)

Open Access Programme (Q4/2026)

Accelerator: Form factor matters!

- Operating a single-device “Alt.1” Accelerator in a PCIe slot of a standard-sized “mid-Tower” workstation case.
- Ongoing: Host-side **multi-device** support.



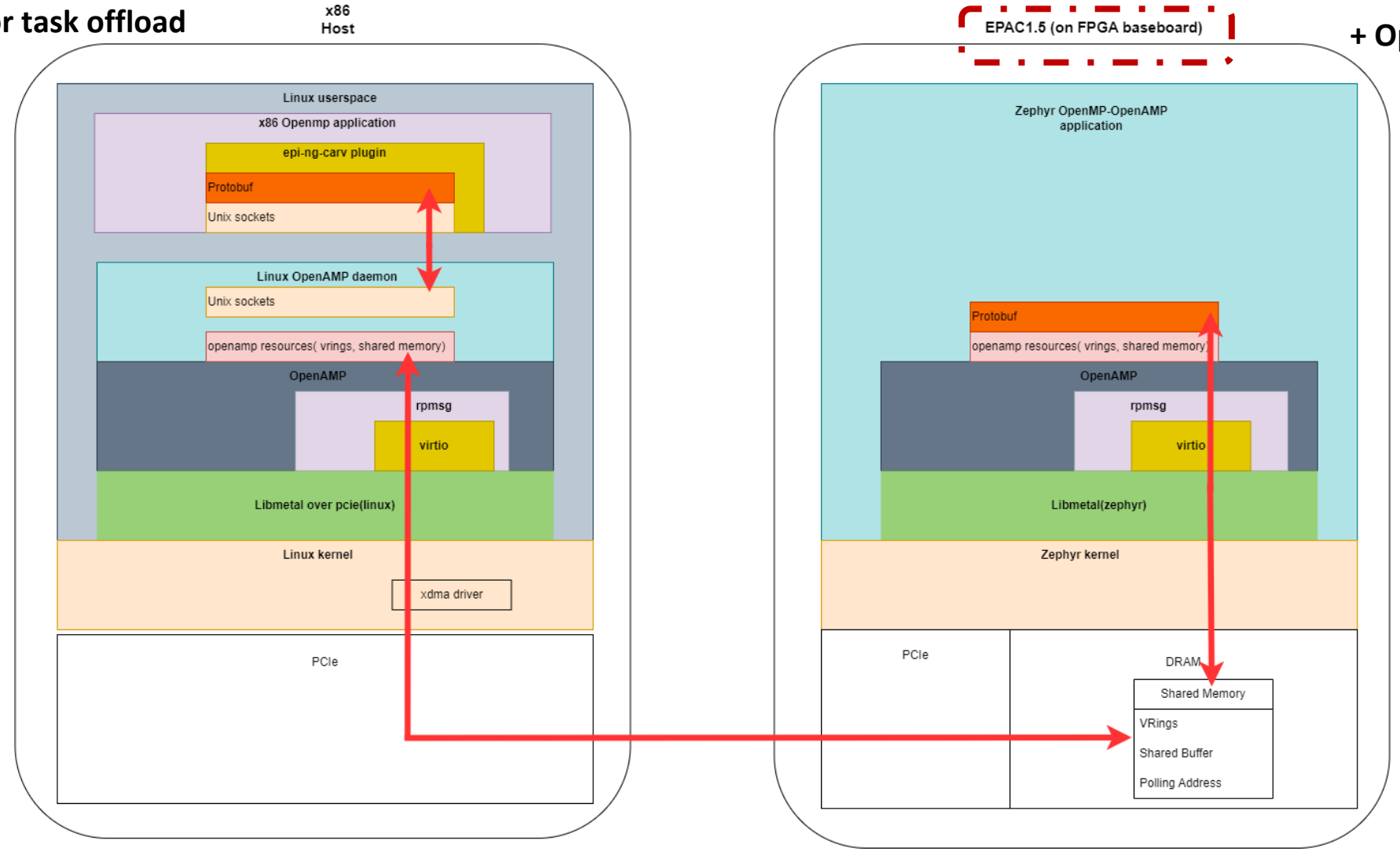
- Still working on dual-device “Alt.1” Accelerator System, i.e. using two PCIe slots of a standard-sized server case.
- **Misc. integration issues**. (esp. PCIe root-complex “nuances”)

Accelerator: System Software

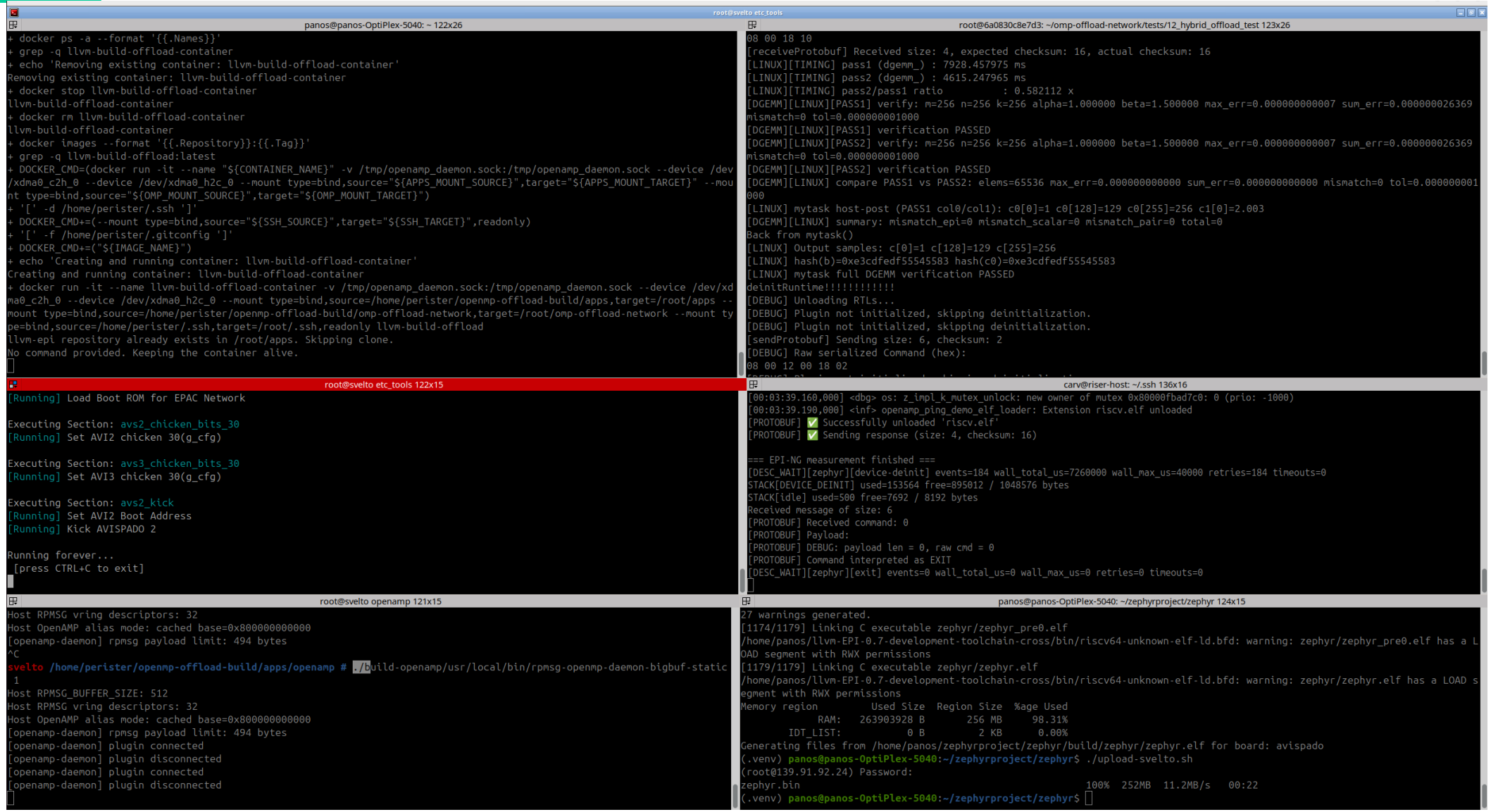
LLVM vectorising compiler (from EPI)
+ OpenMP plugin for task offload

Coming up: Arm Host

RTOS (Zephyr) executor
+ OpenAMP framework

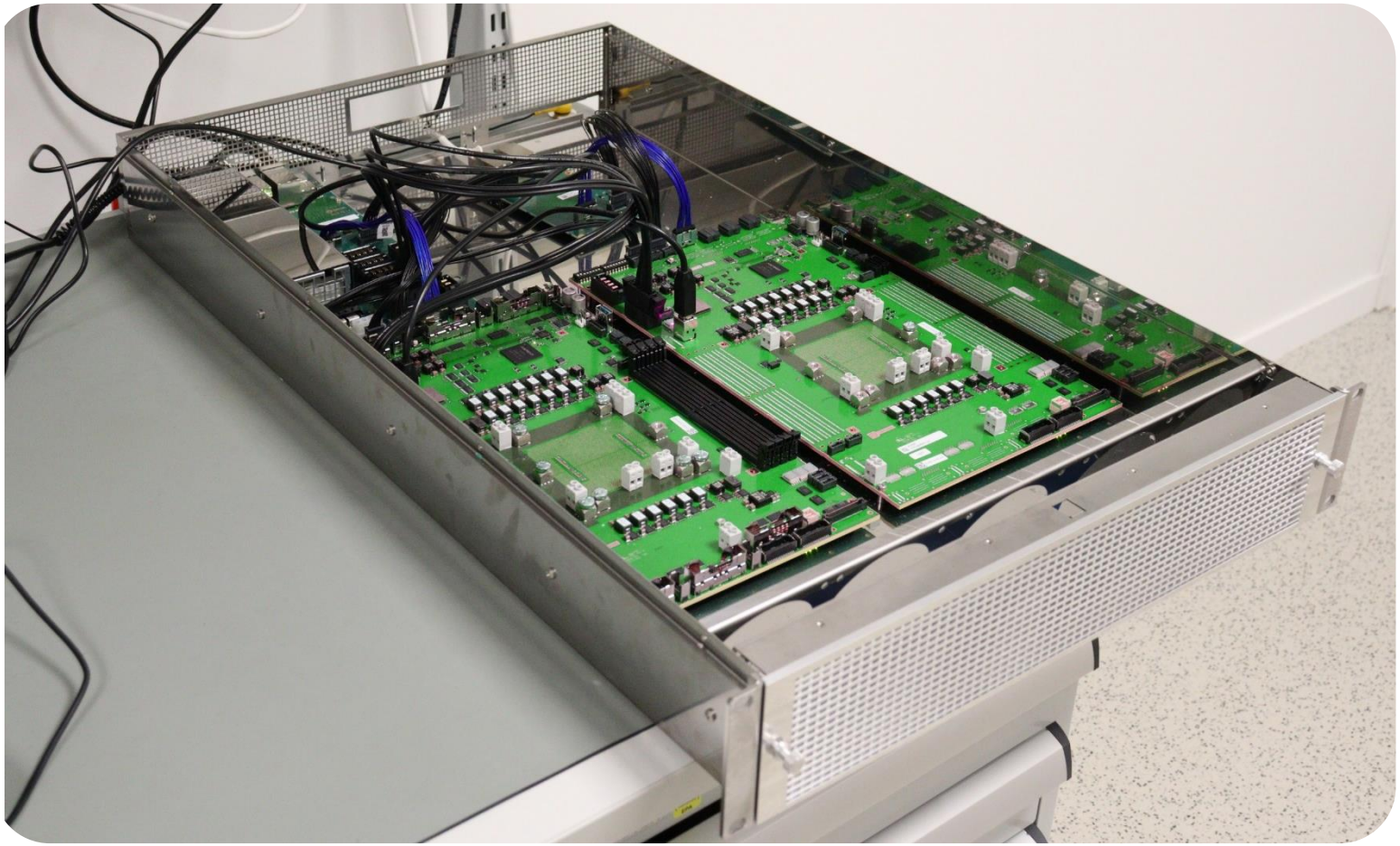


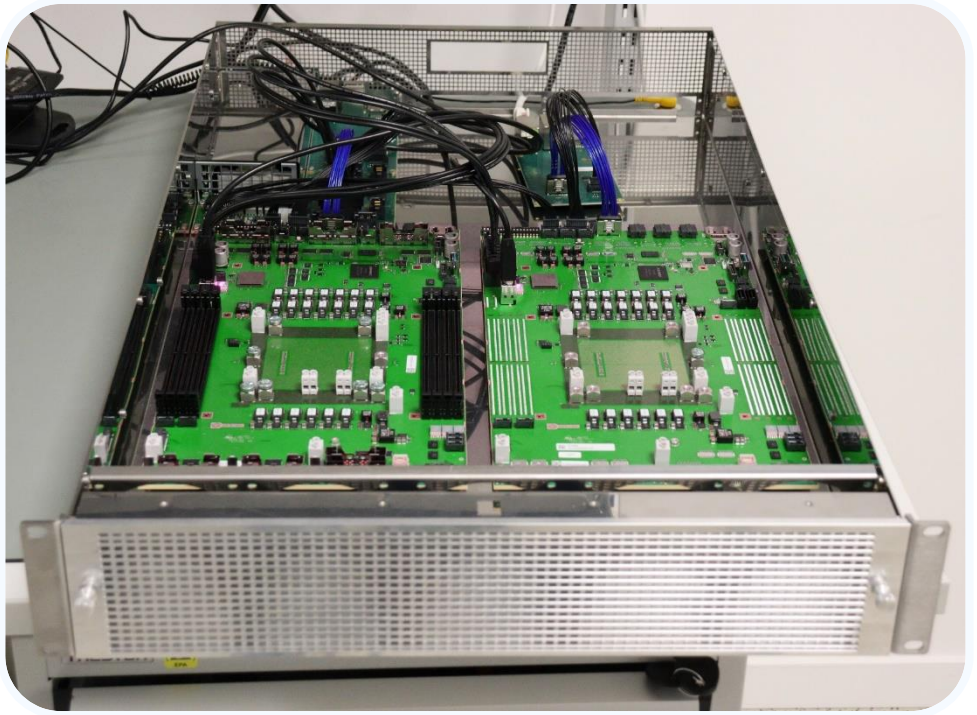
Arm (Radxa Orion O6) → RISC-V (EPAC1.5)



Accelerator Host: SiPEARL's Seine

Rhea1 Arm SoC
(June'2026)





Host prototype to receive SiPEARL's Rhea1 Arm SoC (from the EPI project)

Microserver: Chassis

Daughter Card #2: NVM-Express Storage

+ option to connect 2nd NVM-Express device

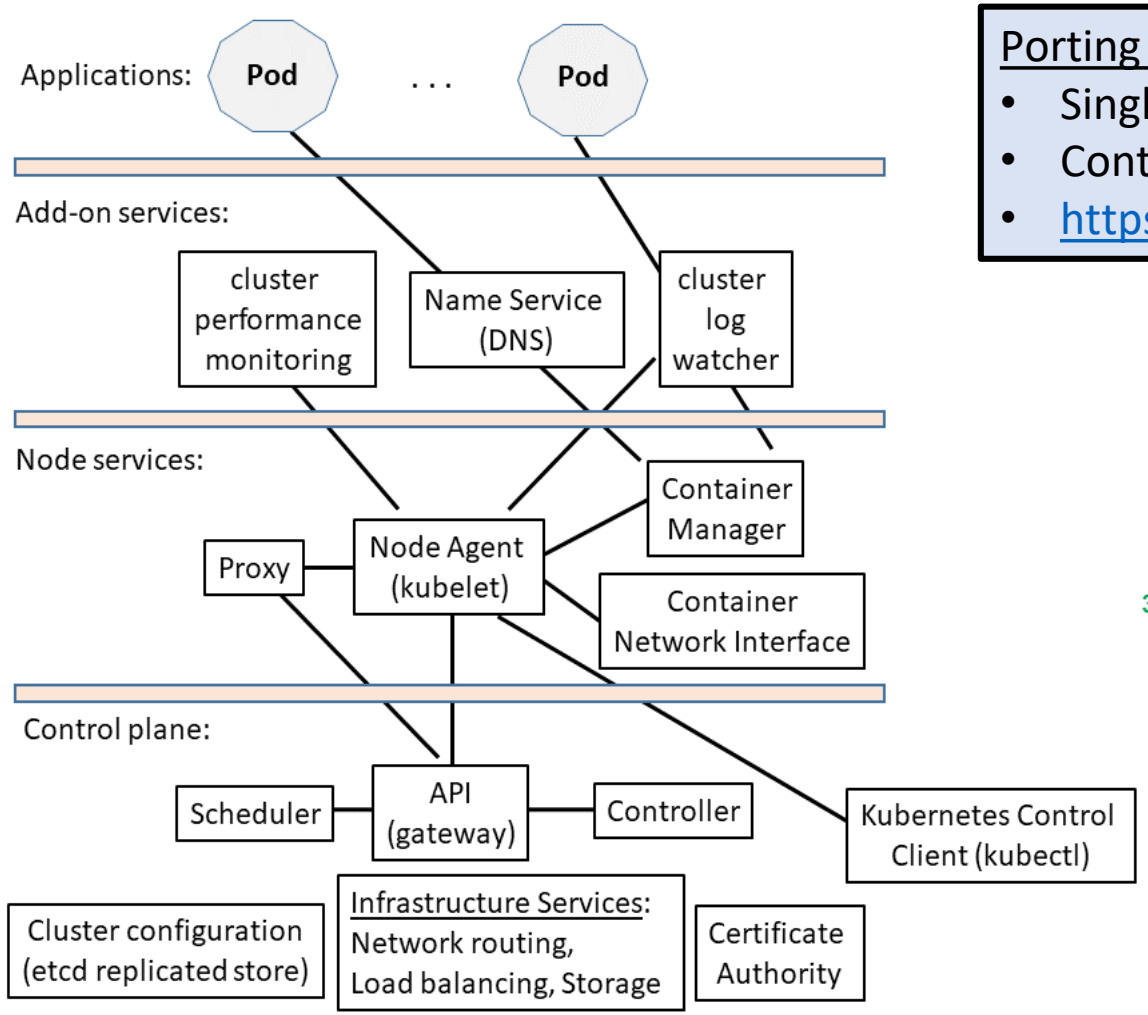
FPGA dev. kit (Baseboard)

Daughter Card #1: EPAC1.5 chip

Mini-ITX:170 mm × 170 mm

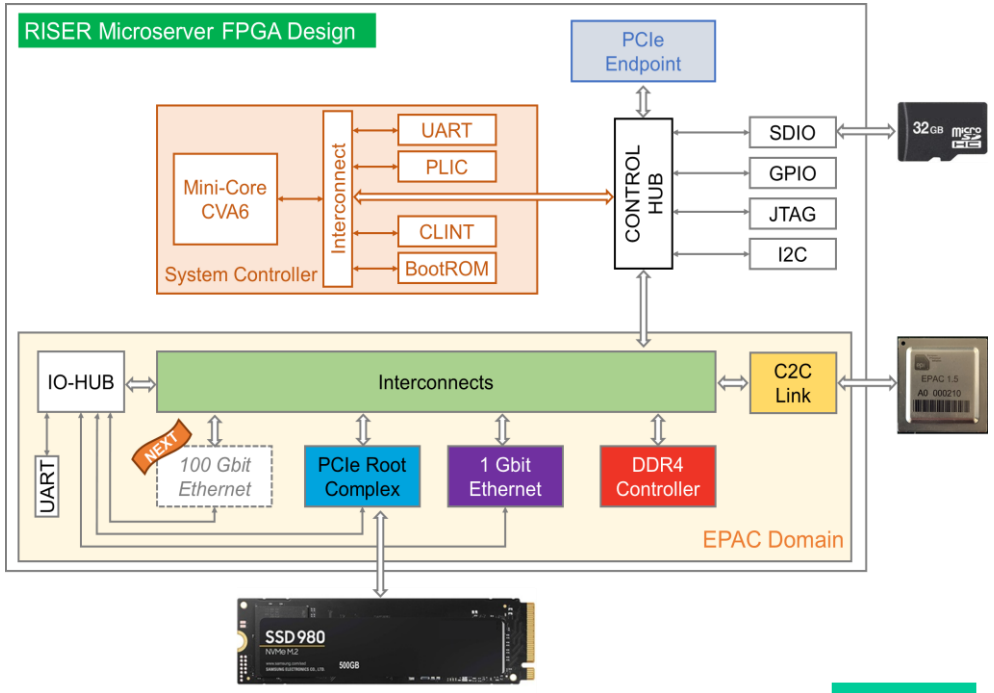
Microserver: Container Services

Container runtime & orchestration: Infrastructure & Node Services, Control Plane



Porting the K3S Kubernetes distribution to RISC-V

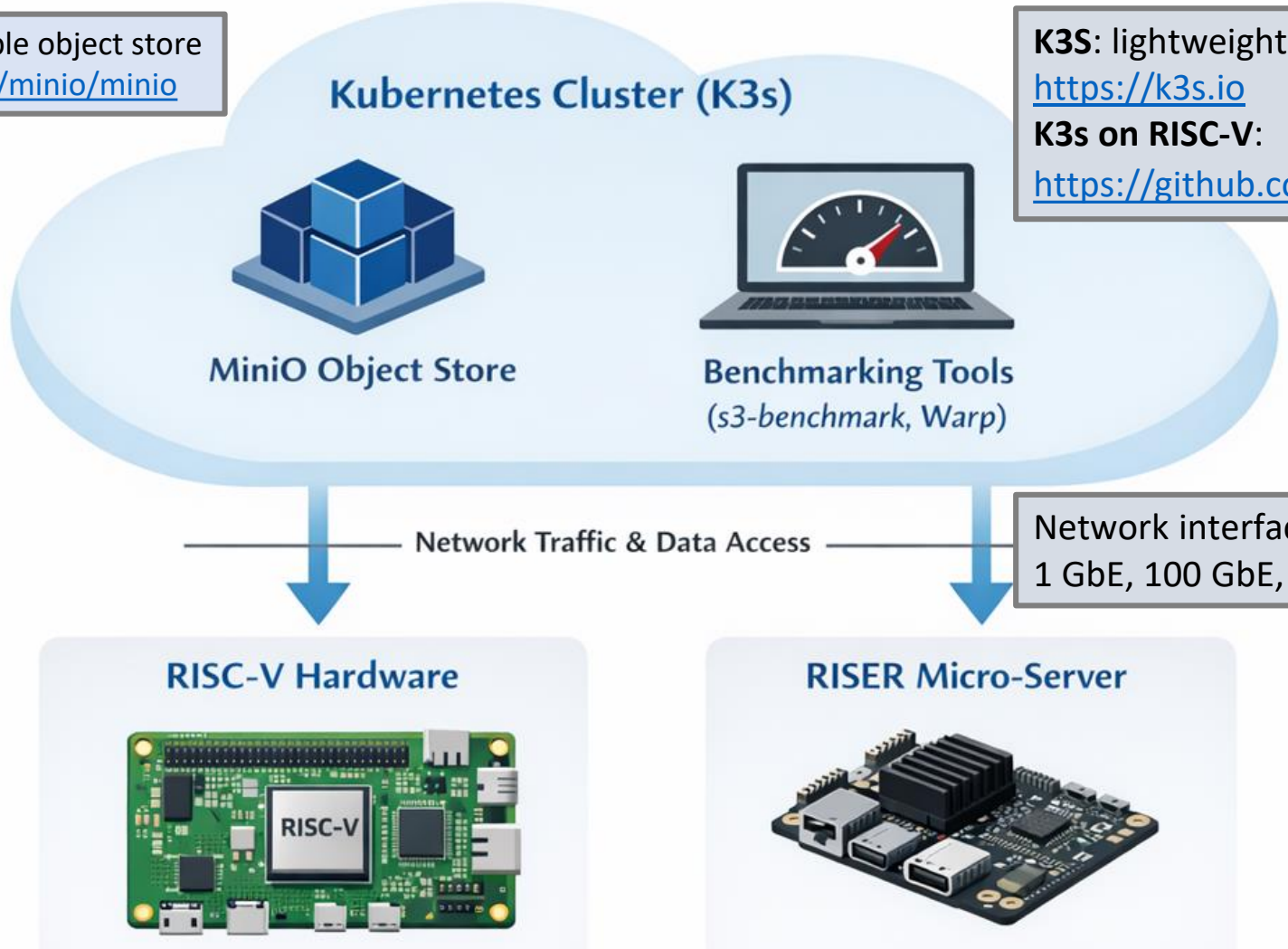
- Single binary for essential Kubernetes services, for easier deployment
- Contributions (PRs) to upstream open-source projects
- https://github.com/CARV-ICS-FORTH/kubernetes-riscv64



Use Case: Networked Object Store

MinIO: S3 compatible object store
https://github.com/minio/minio

K3S: lightweight Kubernetes distribution
https://k3s.io
K3s on RISC-V:
https://github.com/CARV-ICS-FORTH/kubernetes-riscv64



Network interface capability progression:
1 GbE, 100 GbE, RDMA (proprietary …)

Graduation from dev.kit (ISA & SoC compatibility, minimal SW stack) to microserver (high-speed I/O peripherals, full SW stack)

Are we there yet ?

High-end chips are HARD. Schedules and Supply Chains are complex.

Design + Verification + Integration …

- Accelerators

Gaps in availability and integration of suitable IP blocks (incl. Host + Accelerator interaction support, via open-standard HW and SW interfaces)

- Servers

Gaps in availability and integration of suitable IP blocks (incl. efficient use of high-speed I/O peripherals, and open-standard fully-featured SW stacks operating in actual Data Center setting)

My personal view is a _qualified_ but confident YES.

- Many technical and administrative challenges have been overcome.
- On-track to achieve technical goals with impact well outside the project's boundaries.

→ We should also have a roadmap for advanced DC systems as well !

HIGHER (RISER's continuation)

European Heterogeneous Cloud/Edge Infrastructures for Next Generation Hybrid Services

Higher

www.higher-project.eu

Coordination by FORTH INSTITUTE OF COMPUTER SCIENCE

European Heterogeneous Cloud / Edge Infrastructures for Next Generation Hybrid Services

HIGHER aims to prototype and demonstrate the first all-European data center-ready processor and management modules and integrate them into cloud and edge infrastructures using European technologies and Open Compute Project (OCP) standards. HIGHER will adhere to the OCP Data Center Stack (DC-Stack) family of standards, aiming to provide data center-ready integrated systems for edge, private cloud, and large-scale data centers.

Following the OCP Data Center – Modular Hardware System (DC-MHS) specifications for modules compatible across servers, chassis and vendors, HIGHER will develop the following hardware modules:

1. **Processor Modules**: Two OCP-compliant processor modules, which will be based on the OCP Host Processor Module (HPM) or the OCP Universal Baseboard (UBB) standard, one hosting an Arm chip (SiPEARL's Rhea2, derived from the EPI project) and the other hosting a RISC-V chip (VEC, from the EUPILOT project).
2. **Management Module**: A Data Center-ready Secure Control Module (DC-SCM), hosting a RISC-V processor inside an FPGA-based board for server management, security, and control functionality.

Use cases of HIGHER platforms capabilities:

a. Accelerated data processing and analysis;
b. Infrastructure as a Service;
c. Platform as a Service;
d. Remote CXL-based disaggregated memory.

Integrated all-European Hardware & Open-Source Software for Cloud Services and Applications

OCP Server Rack

OCP Server Chassis

OS + Drivers + Runtime

OCP Processor Module Arm SoC (from EPI) + Memory

OCP Processor Module RISC-V SoC (from EUPILOT) + Memory

FW, RoT, BMC

OCP DC-SCM Module (secure control module)

OCP NIC (network interface)

Firmware & Low-Level System Software for Secure Boot, Attestation, Management

DC-SCM

HPM

HIGHER intends to:

- Provide Linux OS and driver support for the OCP compute modules, while creating appropriate software sets for them.
- Provide firmware and system software support for the management module. The management module will be built and expand OpenTitan, an open-source Root-of-Trust project, incorporating a RISC-V core together with hardware and software elements for secure measurements, signature checks, and key management. This is crucial functionality for supporting secure boot and remote attestation procedures for the HIGHER processor modules.
- Incorporate a Meta-OS, i.e. middleware to the software stack for facilitating efficient data processing, storage, and networking across a distributed computing continuum comprising IoT, Edge, and Cloud platforms.

HIGHER: European Heterogeneous Cloud/Edge Infrastructures for Next Generation Hybrid Services
Grant Agreement: 101189612, DG/Agency: HaDEA
Start / end date: 01.01.2025 - 31.12.2027

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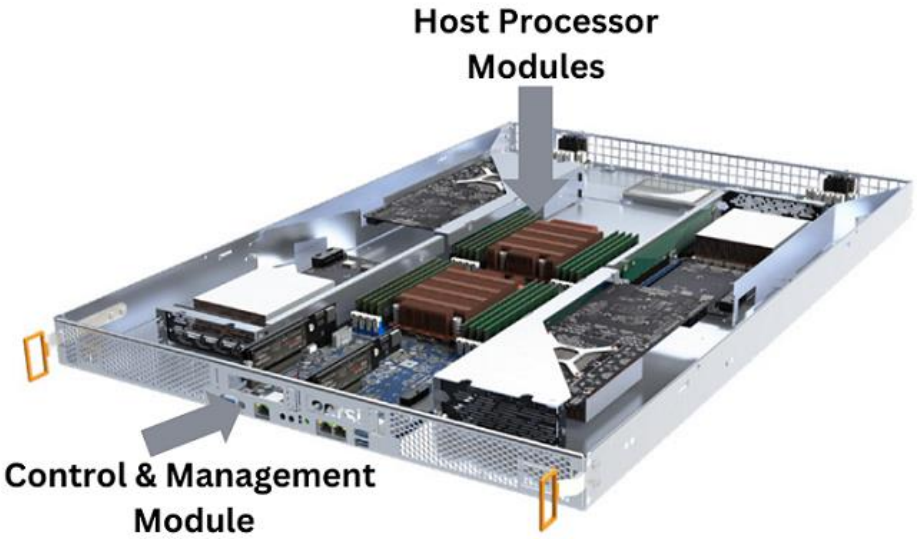
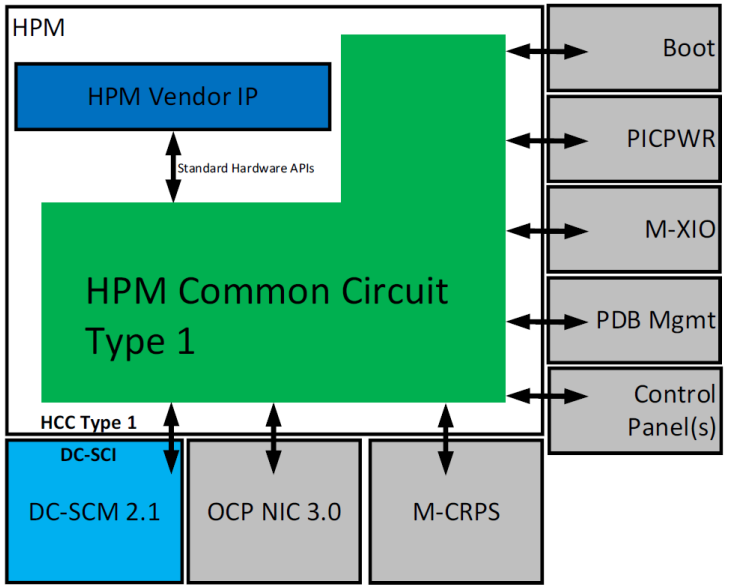
FORTH - Institute of Computer Science, GREECE

Horizon Europe 2021-2027

RISE, EXTOLL, 2crsi, SIPEARL, CloudSigma, eviden, dynamic, BSC, FORTH, EuroHPC JU

- **Open Compute Project → "recipes" for data-centre systems**
- **HIGHER -> Data-centre ready processor (Arm, RISC-V) & management modules based on OCP (HPM, DC-SCM)**





Key themes: Cloud, Edge, ARM, RISC-V, Computing Continuum, Computing for servers, data centres, Open Source Software

HIGHER (GA 101189612 / DG/Agency: HADEA): https://higher-project.eu

[RIA Project started on Jan. 1, 2025]

Closing remarks

- RISER has shown that a RISC-V-based Linux server for cloud services is achievable with European technology.
- HIGHER takes this further by targeting OCP-compliant data center modules—both Arm-based using SiPEARL's Rhea and RISC-V-based using EUPILOT silicon.

- High-end chips are hard. Schedules slip. Supply chains are complex. We should not underestimate the difficulty of what remains.

- **IMHO** : *The question is whether we can sustain the commitment to see it through to production-ready, commercially viable systems.*

Thank you for your attention

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