



Towards European RISC-V Systems: Integration Experiences from the RISER Project

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RISC-V Summit Europe 2026 - Workshop
on “Advancing RISC-V Adoption in HPC
and Cloud Environments”



12th of June, 2026

Project Mission Statement

Can we design and build data-center system platforms based on open standards in Europe today?

Open standards for ISA

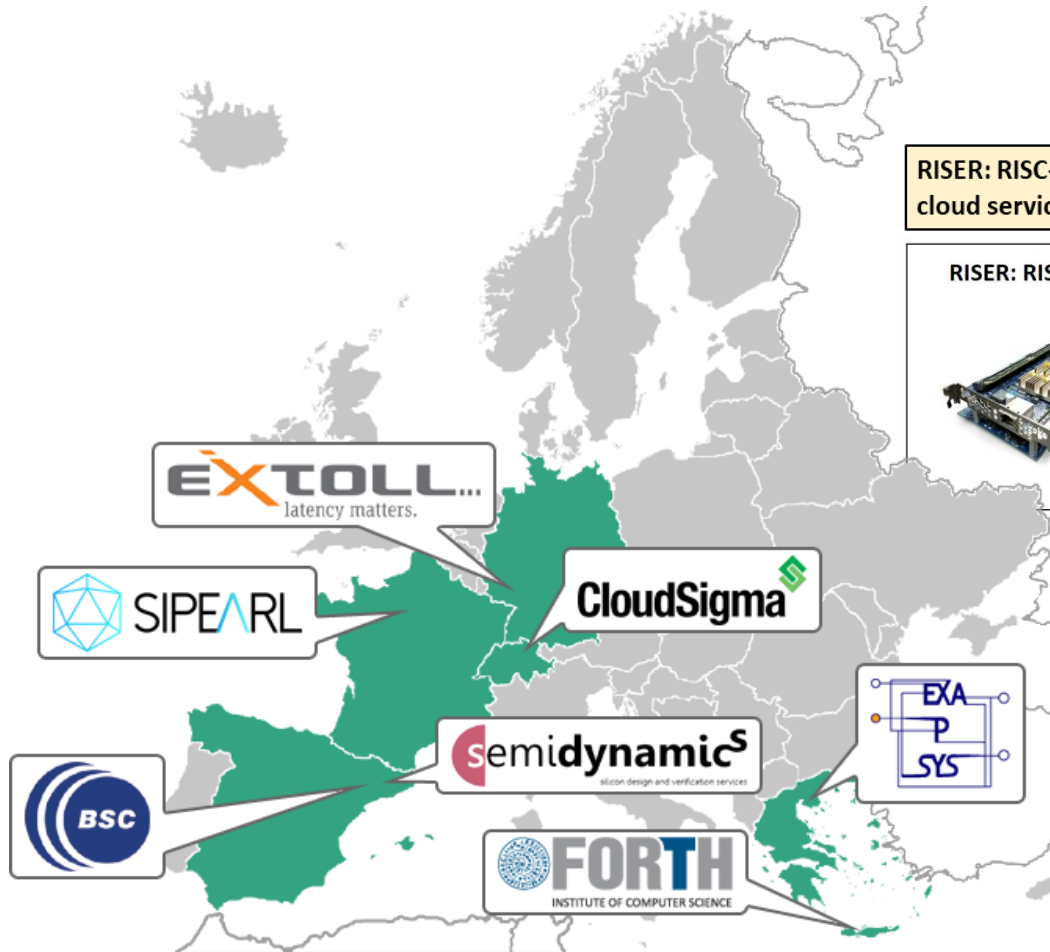


+ Arm ISA (sovereignty-focused projects funded by EuroHPC Joint Undertaking, mainly for HPC)

+ Cloud infrastructure roadmap

RISER in a nutshell

<https://zenodo.org/communities/riser/records>



RISER: RISC-V based Linux server for cloud services, built on open interfaces

RISER: RISC-V for Cloud Services



RISC-V Processors

Source: EPI and EUPilot projects (chips)
* Currently operating on system boards designed for dev/test purposes

Server Boards (PCB + firmware)

Standard form factors (PCIe accelerator card, Microserver)
* Following industry standards to utilize server I/O peripherals

DRAM Memory

NVM-Express Storage

100 Gbps Ethernet

Boot Firmware

Initialization of execution platform, Including high-speed I/O peripherals (storage, networking)

OS, drivers, runtime

Configured/adapted for cloud services: workload acceleration, networked storage, containerized execution
* Integration in IaaS environment

<https://riser-project.eu>

<https://www.linkedin.com/company/riser-project/>

<https://twitter.com/RiserProject>

Integrated all-European Hardware and Open-Source Software for Cloud Services and Applications

12th of June, 2026

RISC-V Summit Europe 2026 - Workshop

[RIA Project started on Jan. 1, 2023]

- Chips from the EPI project → basis of platform prototypes

- **Host-Accelerator**

- Host: Arm HPC SoC, by SiPEARL
- Accelerator: RISC-V SoC, with the Avispado core by Semidynamics

- **Microserver**

- Standalone (FPGA-assisted), using RISC-V SoC
- upcoming: variant based RISC-V SoC from the EUPILLOT project

- Open-source designs, incl. Firmware, OS, runtimes

- Use cases:

- **Acceleration: OpenMP multi-device task offload**
- **Cloud: Containers & Orchestration (Kubernetes) runtime, IaaS, Networked Storage**



EPAC1.5 (from EPI-SGA2)

EPAC1.5 test-chip from EPI.

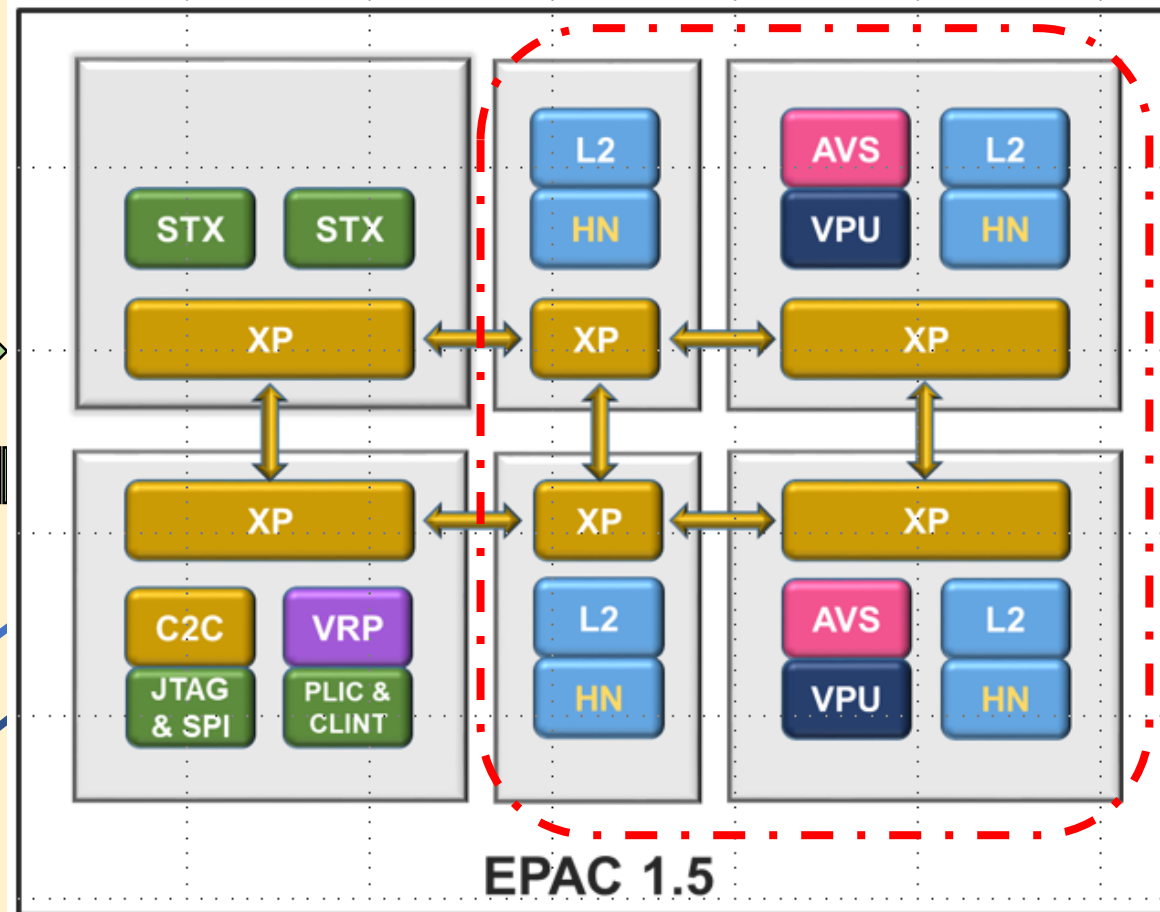
- No on-chip Memory & PCIe controllers
- Requires external Config/Boot

Development Host:

- JTAG (for reset/control)
- PCIe controller for loading FPGA memories with boot images

EXTOLL NoC
Cross-Points
& Chip-to-Chip links

FPGA Board (Memory Controller, PCIe endpoint)



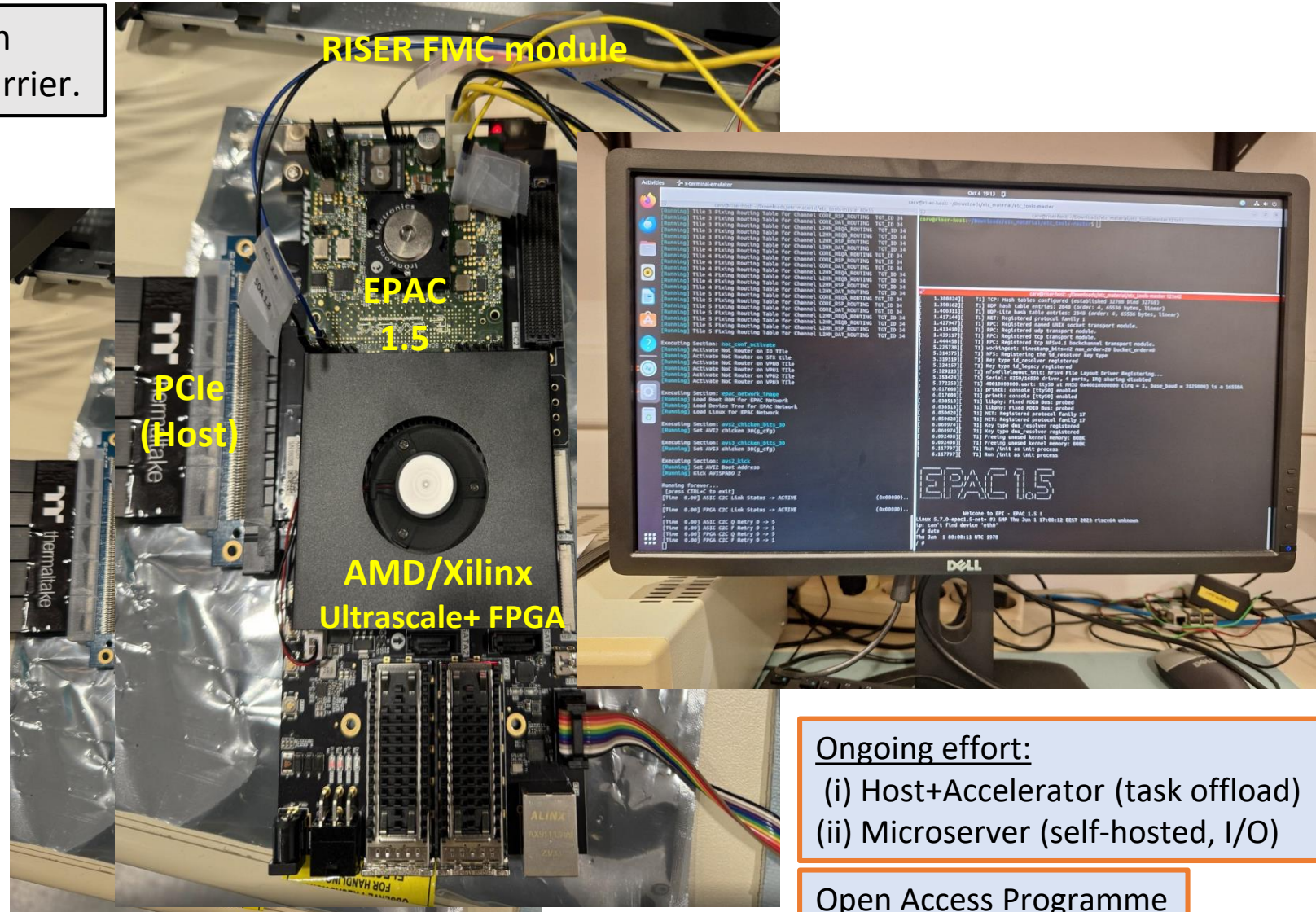
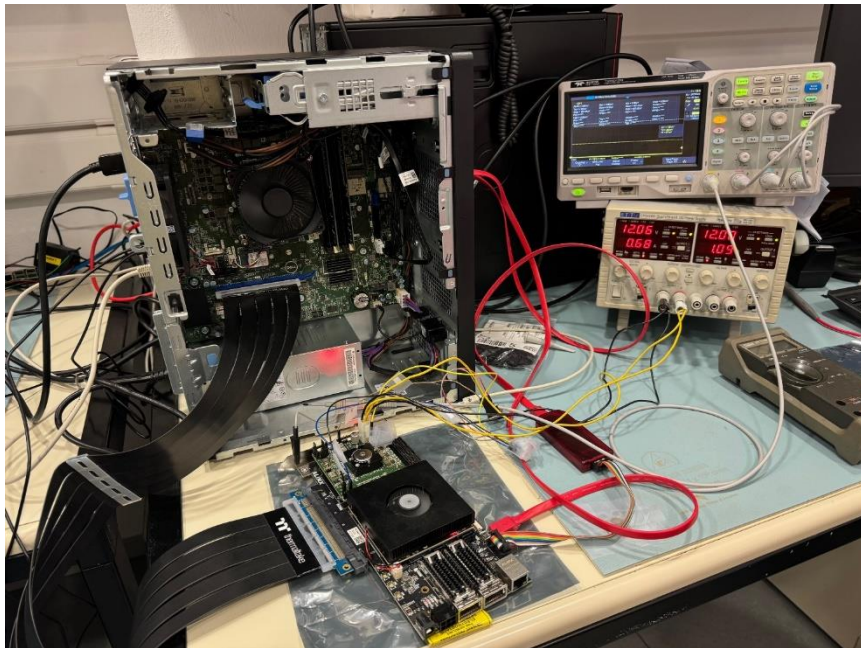
Copyright © European Processor Initiative 2023 EPI-SGA2 Monthly report for M20 – August 2023

SMD RISC-V
+ BSC vector
+ FORTH L2
cache

FPGA (FMC+)
Daughterboard

Prototypes using test-chip from EPI

PCIe-hosted Accelerator: test-chip hosted on miniaturized FMC daughtercard on FPGA carrier.



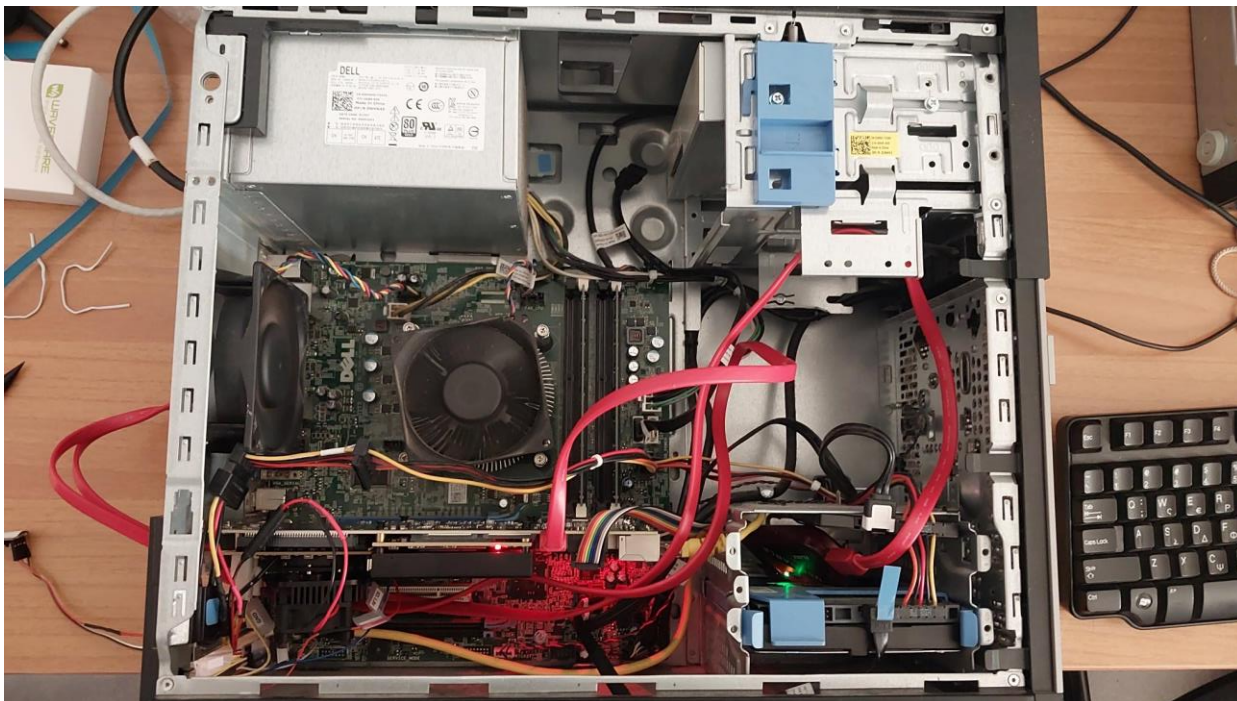
Ongoing effort:

- (i) Host+Accelerator (task offload)
- (ii) Microserver (self-hosted, I/O)

Open Access Programme
(Q4/2026)

Accelerator: Form factor matters!

- Operating a single-device “Alt.1” Accelerator in a PCIe slot of a standard-sized “mid-Tower” workstation case.
- Ongoing: Host-side **multi-device** support.



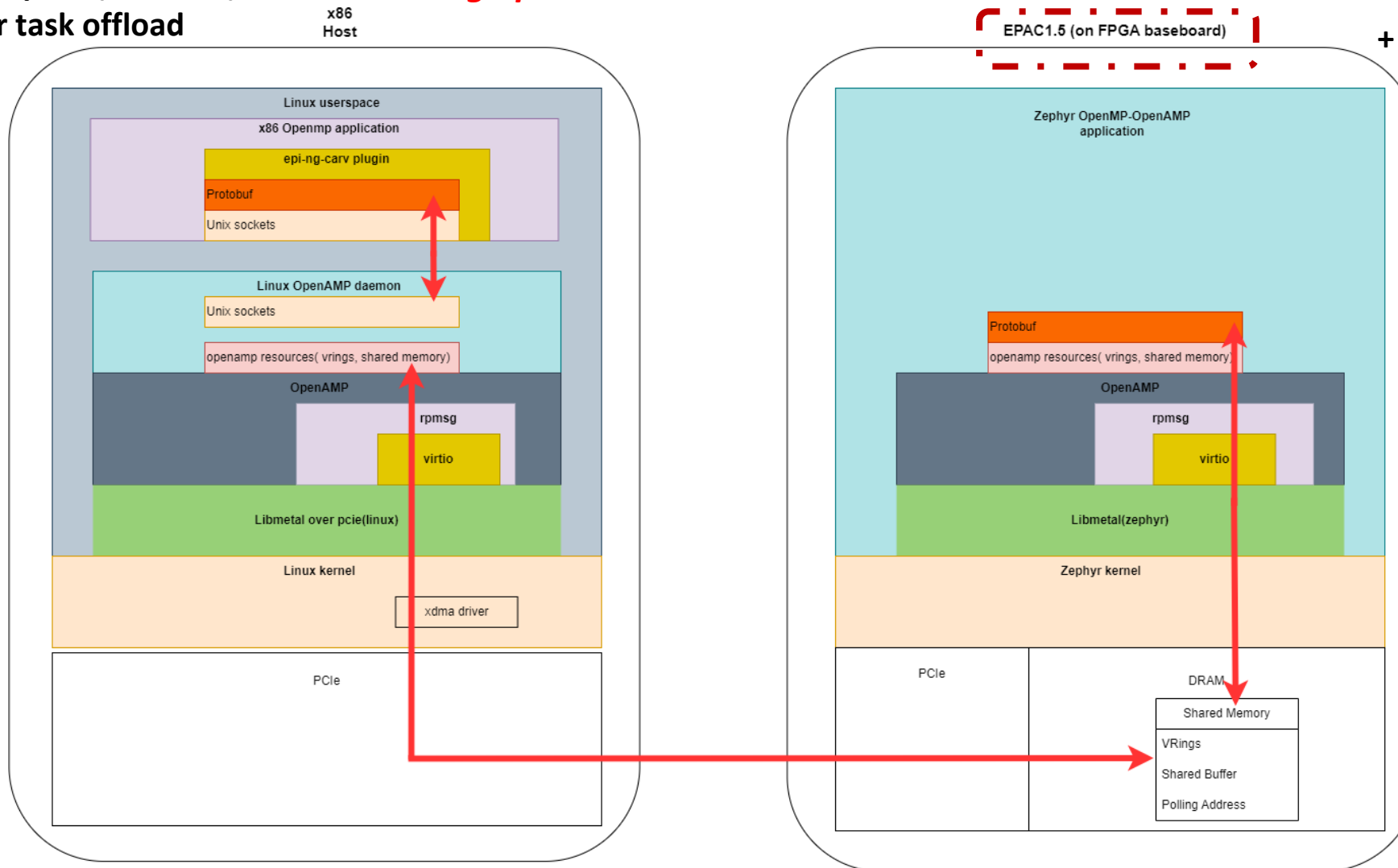
- Still working on dual-device “Alt.1” Accelerator System, i.e. using two PCIe slots of a standard-sized server case.
- **Misc. integration issues**. (esp. PCIe root-complex “nuances”)

Accelerator: System Software

LLVM vectorising compiler (from EPI)
+ OpenMP plugin for task offload

Coming up: Arm Host

RTOS (Zephyr) executor
+ OpenAMP framework





Arm (Radxa Orion O6) → RISC-V (EPAC1.5)

```
panos@panos-OptiPlex-5040: ~ 122x26
+ docker ps -a --format '{{.Names}}'
+ grep -q llvm-build-offload-container
+ echo 'Removing existing container: llvm-build-offload-container'
Removing existing container: llvm-build-offload-container
+ docker stop llvm-build-offload-container
llvm-build-offload-container
+ docker rm llvm-build-offload-container
llvm-build-offload-container
+ docker images --format '{{.Repository}}:{{.Tag}}'
+ grep -q llvm-build-offload:latest
+ DOCKER_CMD=(docker run -it --name "${CONTAINER_NAME}" -v /tmp/openamp_daemon.sock:/tmp/openamp_daemon.sock --device /dev
/xdma0_c2h_0 --device /dev/xdma0_h2c_0 --mount type=bind,source="${APPS_MOUNT_SOURCE}",target="${APPS_MOUNT_TARGET}" --mou
nt type=bind,source="${OMP_MOUNT_SOURCE}",target="${OMP_MOUNT_TARGET}")
+ '[' -d /home/perister/.ssh ']'
+ DOCKER_CMD+=(-m mount type=bind,source="${SSH_SOURCE}",target="${SSH_TARGET}",readonly)
+ '[' -f /home/perister/.gitconfig ']'
+ DOCKER_CMD+=("${IMAGE_NAME}")
+ echo 'Creating and running container: llvm-build-offload-container'
Creating and running container: llvm-build-offload-container
+ docker run -it --name llvm-build-offload-container -v /tmp/openamp_daemon.sock:/tmp/openamp_daemon.sock --device /dev/xd
ma0_c2h_0 --device /dev/xdma0_h2c_0 --mount type=bind,source=/home/perister/openmp-offload-build/apps,target=/root/apps --
mount type=bind,source=/home/perister/.ssh,target=/root/.ssh,readonly llvm-build-offload
llvm-epi repository already exists in /root/apps. Skipping clone.
No command provided. Keeping the container alive.

root@svelto etc.tools 122x15
[Running] Load Boot ROM for EPAC Network

Executing Section: avs2_chicken_bits_30
[Running] Set AVI2 chicken 30(g_cfg)

Executing Section: avs3_chicken_bits_30
[Running] Set AVI3 chicken 30(g_cfg)

Executing Section: avs2_kick
[Running] Set AVI2 Boot Address
[Running] Kick AVISPAD0 2

Running forever...
[press CTRL+C to exit]

root@svelto openamp 121x15
Host RPMSG wring descriptors: 32
Host OpenAMP alias mode: cached base=0x800000000000
[openamp-daemon] rpmsg payload limit: 494 bytes
^C
svelto /home/perister/openmp-offload-build/apps/openamp # ./build-openamp/usr/local/bin/rpmsg-openamp-daemon-bigbuf-static
1
Host RPMSG_BUFFER_SIZE: 512
Host RPMSG wring descriptors: 32
Host OpenAMP alias mode: cached base=0x800000000000
[openamp-daemon] rpmsg payload limit: 494 bytes
[openamp-daemon] plugin connected
[openamp-daemon] plugin disconnected
[openamp-daemon] plugin connected
[openamp-daemon] plugin disconnected

root@6a0830c8e7d3: ~/omp-offload-network/tests/12_hybrid_offload_test 123x26
08 00 18 10
[receiveProtobuf] Received size: 4, expected checksum: 16, actual checksum: 16
[LINUX][TIMING] pass1 (dgemm_) : 7928.457975 ms
[LINUX][TIMING] pass2 (dgemm_) : 4615.247965 ms
[LINUX][TIMING] pass2/pass1 ratio : 0.582112 x
[DGEMM][LINUX][PASS1] verify: m=256 n=256 k=256 alpha=1.000000 beta=1.500000 max_err=0.000000000007 sum_err=0.000000026369
mismatch=0 tol=0.000000001000
[DGEMM][LINUX][PASS1] verification PASSED
[DGEMM][LINUX][PASS2] verify: m=256 n=256 k=256 alpha=1.000000 beta=1.500000 max_err=0.000000000007 sum_err=0.000000026369
mismatch=0 tol=0.000000001000
[DGEMM][LINUX][PASS2] verification PASSED
[DGEMM][LINUX] compare PASS1 vs PASS2: elems=65536 max_err=0.000000000000 sum_err=0.000000000000 mismatch=0 tol=0.000000001
000
[LINUX] mytask host-post (PASS1 col0/col1): c0[0]=1 c0[128]=129 c0[255]=256 c1[0]=2.003
[DGEMM][LINUX] summary: mismatch_epi=0 mismatch_scalar=0 mismatch_pair=0 total=0
Back from mytask()
[LINUX] Output samples: c0[0]=1 c0[128]=129 c0[255]=256
[LINUX] hash(b)=0xe3cdfedf55545583 hash(c0)=0xe3cdfedf55545583
[LINUX] mytask full DGEMM verification PASSED
deinitRuntime!!!!!!!!!!!!
[DEBUG] Unloading RTLs...
[DEBUG] Plugin not initialized, skipping deinitialization.
[DEBUG] Plugin not initialized, skipping deinitialization.
[sendProtobuf] Sending size: 6, checksum: 2
[DEBUG] Raw serialized Command (hex):
08 00 12 00 18 02

carv@riser-host: ~/ssh 136x16
[00:03:39.160,000] <dbg> os: z_impl_k_mutex_unlock: new owner of mutex 0x80000fbad7c0: 0 (prio: -1000)
[00:03:39.190,000] <inf> openamp_ping_demo_elf_loader: Extension riscv.elf unloaded
[PROTOBUF] [x] Successfully unloaded 'riscv.elf'
[PROTOBUF] [x] Sending response (size: 4, checksum: 16)

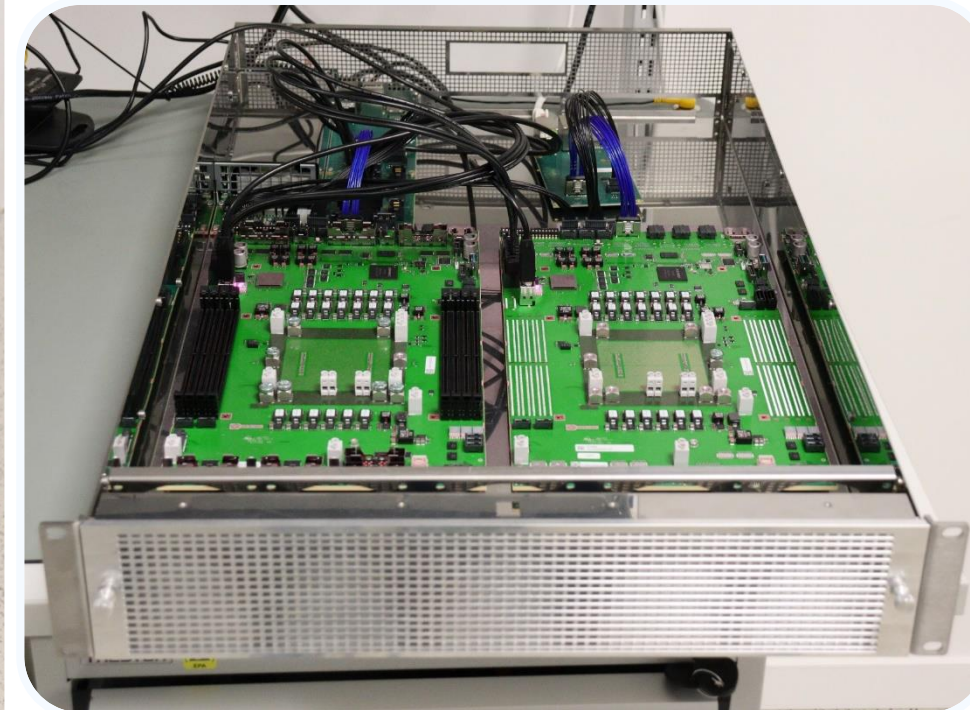
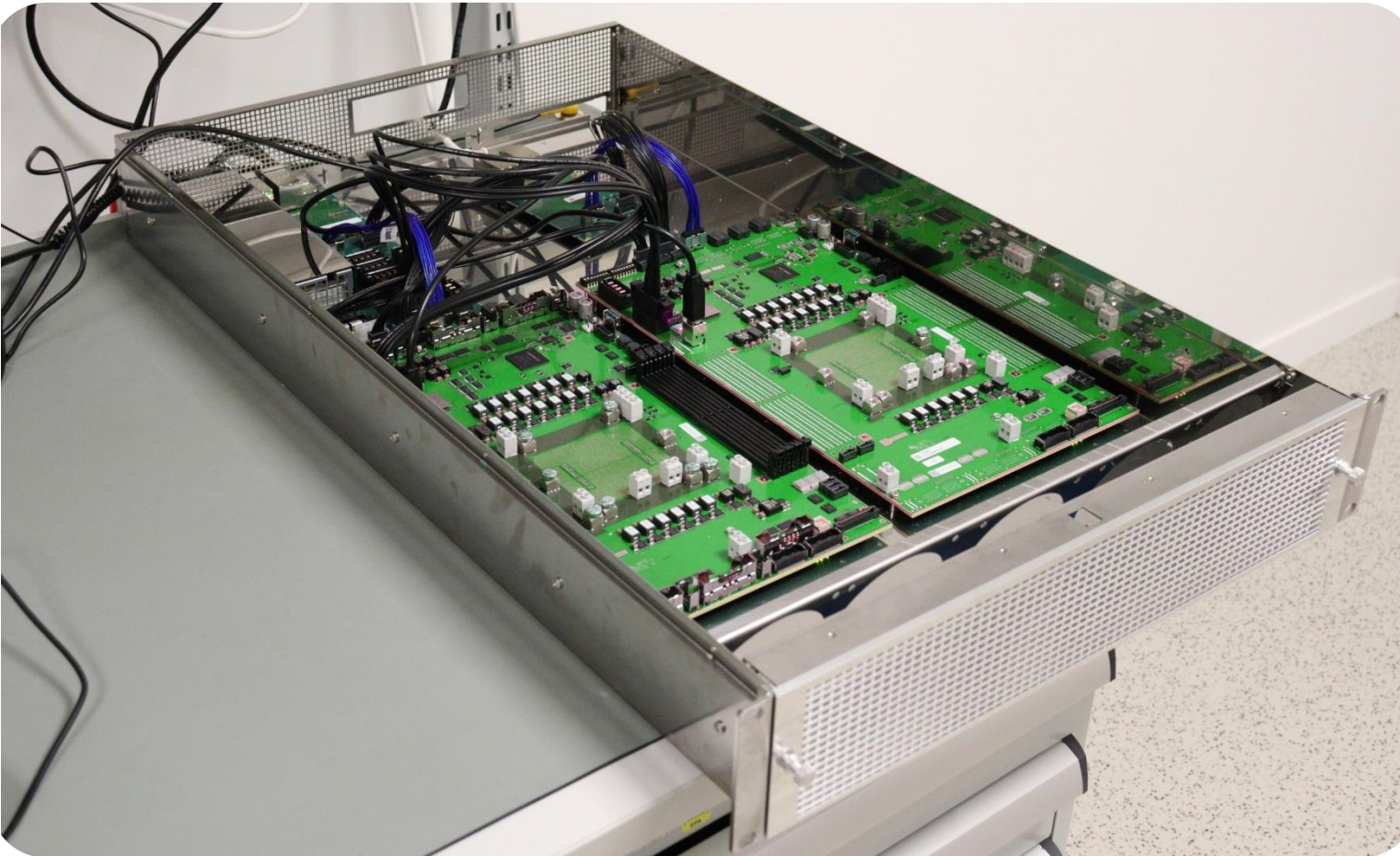
=== EPI-NG measurement finished ===
[DESC_WAIT][zephyr][device-deinit] events=184 wall_total_us=7260000 wall_max_us=40000 retries=184 timeouts=0
STACK[DEVICE_DEINIT] used=153564 free=895012 / 1048576 bytes
STACK[idle] used=500 free=7692 / 8192 bytes
Received message of size: 6
[PROTOBUF] Received command: 0
[PROTOBUF] Payload:
[PROTOBUF] DEBUG: payload len = 0, raw cmd = 0
[PROTOBUF] Command interpreted as EXIT
[DESC_WAIT][zephyr][exit] events=0 wall_total_us=0 wall_max_us=0 retries=0 timeouts=0

panos@panos-OptiPlex-5040: ~/zephyrproject/zephyr 124x15
27 warnings generated.
[1174/1179] Linking C executable zephyr/zephyr_pre0.elf
/home/panos/llvm-EPI-0.7-development-toolchain-cross/bin/riscv64-unknown-elf-ld.bfd: warning: zephyr/zephyr_pre0.elf has a L
OAD segment with RWX permissions
[1179/1179] Linking C executable zephyr/zephyr.elf
/home/panos/llvm-EPI-0.7-development-toolchain-cross/bin/riscv64-unknown-elf-ld.bfd: warning: zephyr/zephyr.elf has a LOAD s
egment with RWX permissions
Memory region      Used Size  Region Size  %age Used
RAM:               263903928 B    256 MB    98.31%
IDT_LIST:           0 B          2 KB     0.00%
Generating files from /home/panos/zephyrproject/zephyr/build/zephyr/zephyr.elf for board: avispado
(.venv) panos@panos-OptiPlex-5040:~/zephyrproject/zephyr$ ./upload-svelto.sh
(root@139.91.92.24) Password:
zephyr.bin               100% 252MB 11.2MB/s 00:22
(.venv) panos@panos-OptiPlex-5040:~/zephyrproject/zephyr$
```

Accelerator Host: SiPEARL's Seine



Rhea1 Arm SoC
(June'2026)



Host prototype to receive
SiPEARL's Rhea1 Arm SoC
(from the EPI project)

Microserver: Chassis

Daughter Card #1:
EPAC1.5 chip

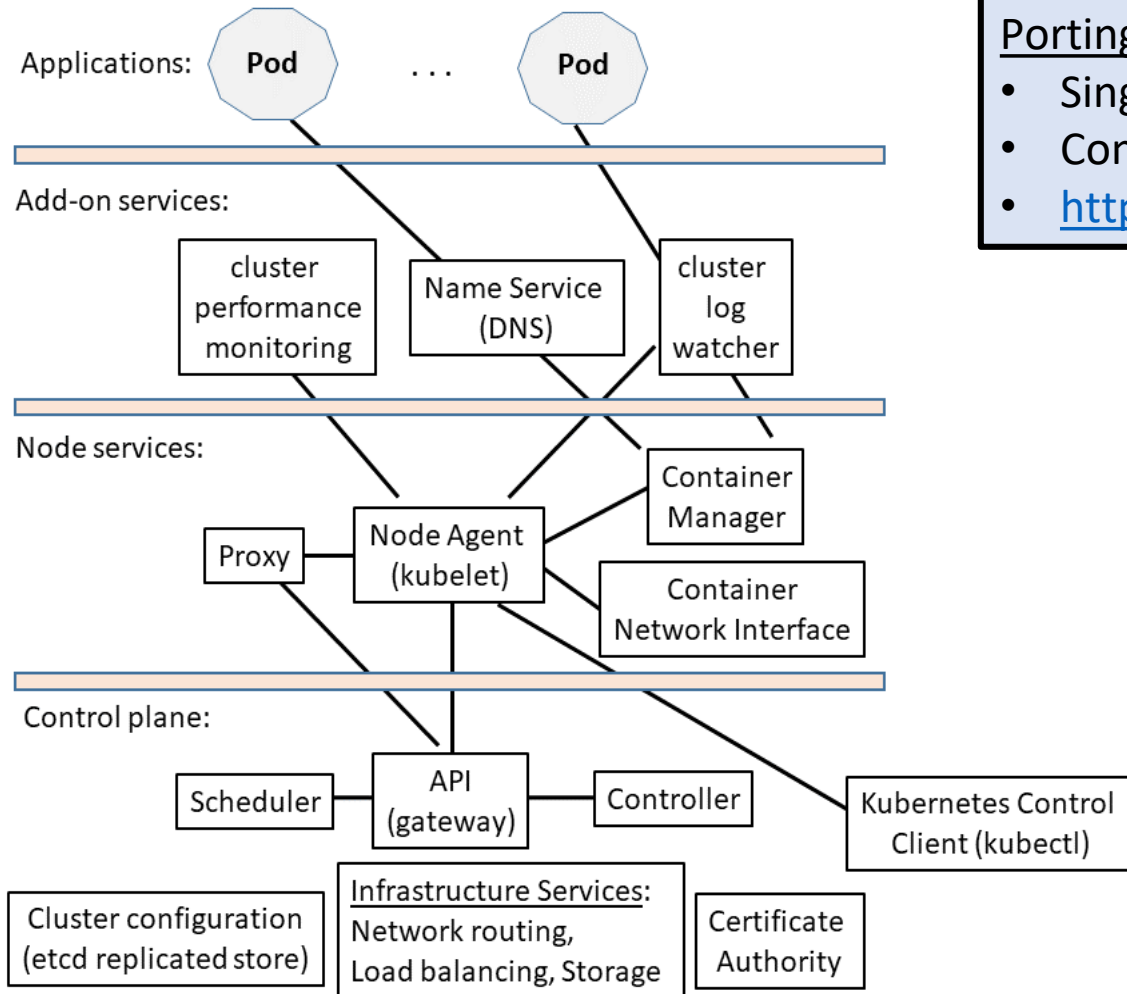
Daughter Card #2:
NVM-Express
Storage + option to connect 2nd
NVM-Express device

FPGA dev. kit
(Baseboard)



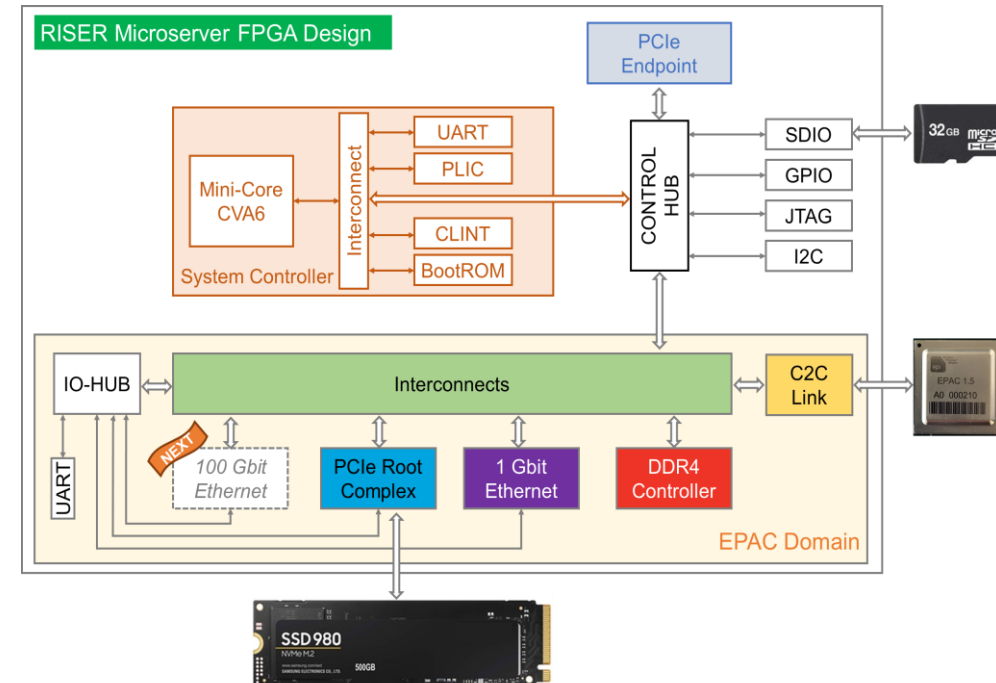
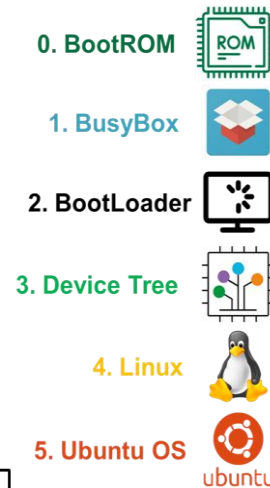
Mini-ITX: 170 mm × 170 mm

Container runtime & orchestration: Infrastructure & Node Services, Control Plane



Porting the K3S Kubernetes distribution to RISC-V

- Single binary for essential Kubernetes services, for easier deployment
- Contributions (PRs) to upstream open-source projects
- <https://github.com/CARV-ICS-FORTH/kubernetes-riscv64>



Use Case: Networked Object Store

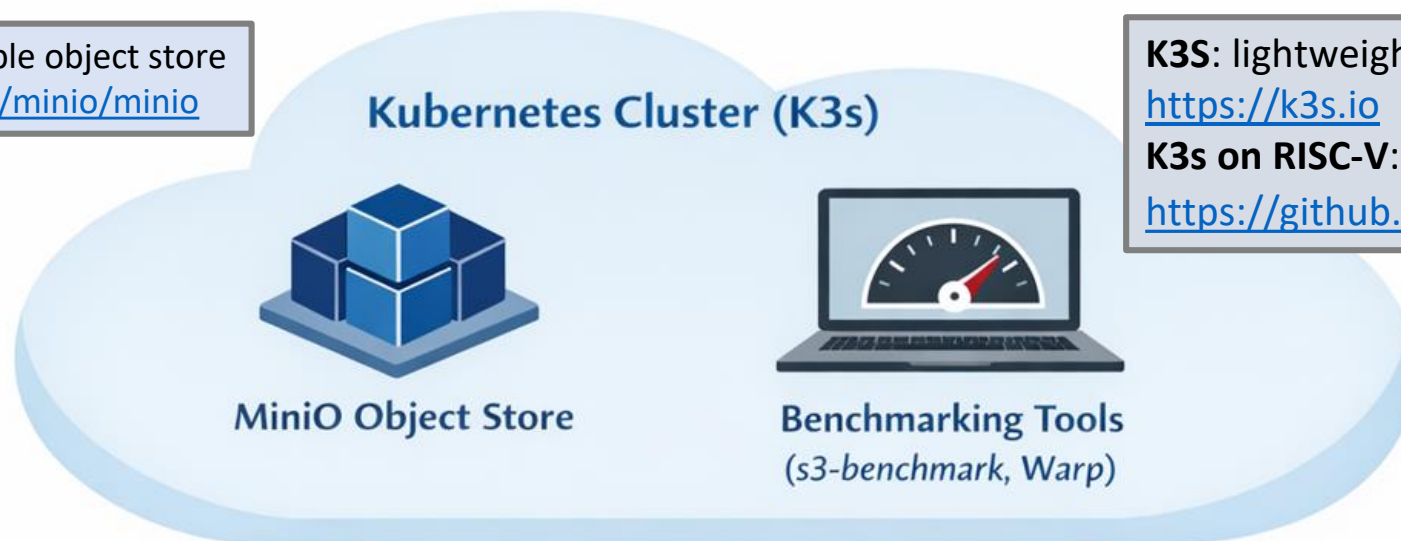
MinIO: S3 compatible object store
<https://github.com/minio/minio>

K3S: lightweight Kubernetes distribution

<https://k3s.io>

K3s on RISC-V:

<https://github.com/CARV-ICS-FORTH/kubernetes-riscv64>



Network Traffic & Data Access

Network interface capability progression:
 1 GbE, 100 GbE, RDMA (proprietary ...)

RISC-V Hardware



RISER Micro-Server



Graduation from dev.kit (ISA & SoC compatibility, minimal SW stack) to microserver (high-speed I/O peripherals, full SW stack)

Are we there yet ?

High-end chips are HARD. Schedules and Supply Chains are complex.

Design + Verification + **Integration** ...

- Accelerators

Gaps in availability and integration of suitable IP blocks (incl. Host + Accelerator interaction support, via open-standard HW and SW interfaces)

- Servers

Gaps in availability and integration of suitable IP blocks (incl. efficient use of high-speed I/O peripherals, and open-standard fully-featured SW stacks operating in actual Data Center setting)

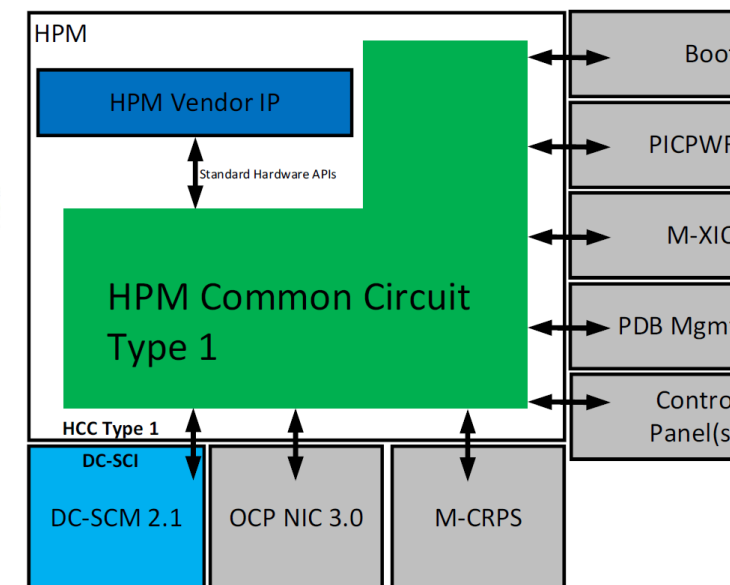
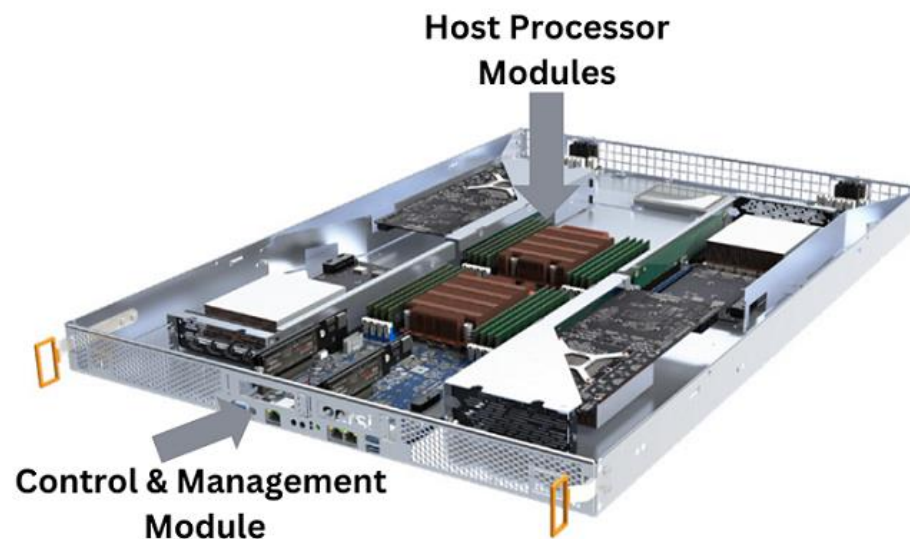
My personal view is a _qualified_ but confident YES.



- Many technical and administrative challenges have been overcome.
- On-track to achieve technical goals with impact well outside the project's boundaries.

→ We should also have a roadmap for advanced DC systems as well !

- Open Compute Project → “recipes” for data-centre systems
- HIGHER -> Data-centre ready processor (Arm, RISC-V) & management modules based on OCP (HPM, DC-SCM)



Key themes: Cloud, Edge, ARM, RISC-V, Computing Continuum, Computing for servers, data centres, Open Source Software

www.higher-project.eu

Coordination by

INSTITUTE OF COMPUTER SCIENCE

European Heterogeneous Cloud / Edge Infrastructures for Next Generation Hybrid Services

HIGHER aims to prototype and demonstrate the first all-European data center-ready processor and management modules and integrate them into cloud and edge infrastructures using European technologies and Open Compute Project (OCP) standards. HIGHER will adhere to the OCP Data Center Stack (DC-Stack) family of standards, aiming to provide data center-ready integrated systems for edge, private cloud, and large-scale data centers.

Following the OCP Data Center – Modular Hardware System (DC-MHS) specifications for modules compatible across servers, chassis and vendors, HIGHER will develop the following hardware modules:

1. **Processor Modules:** Two OCP-compliant processor modules, which will be based on the OCP Host Processor Module (HPM) or the OCP Universal Baseboard (UBB) standard, one hosting an Arm chip (SPEARL's Rhea2, derived from the EPI project) and the other hosting a RISC-V chip (VEC, from the EUPLOTT project).
2. **Management Module:** A Data Center-ready Secure Control Module (DC-SCM), hosting a RISC-V processor inside an FPGA-based board for server management, security, and control functionality.

Use cases of HIGHER platforms capabilities:

- a. Accelerated data processing and analysis;
- b. Infrastructure as a Service;
- c. Platform as a Service;
- d. Remote CXL-based disaggregated memory.

... Integrated all-European Hardware & Open-Source Software for Cloud Services and Applications

OCP Server Stack

OS + Drivers + Runtime	OCP Server Chassis
OCP Processor Module Arm SoC (from BP) + Memory	F/W, RoT, BMC
OCP Processor Module RISC-V SoC (from EUPLOTT) + Memory	OCP DC-SCM Module (Secure Control Module)
	OCP NIC (network interface)

Firmware & User-Level System Software for Secure Boot, Authentication, Management

HIGHER intends to:

- Provide Linux OS and driver support for the OCP compute modules, while creating appropriate software sets for them.
- Provide firmware and system software support for the management module. The management module will be built and expand OpenTitan, an open-source Root-of-Trust project, incorporating a RISC-V core together with hardware and software elements for secure measurements, signature checks, and key management. This is crucial functionality for supporting secure boot and remote attestation procedures for the HIGHER processor modules.
- Incorporate a Meta-OS, i.e. middleware to the software stack for facilitating efficient data processing, storage, and networking across a distributed computing continuum comprising IoT, Edge, and Cloud platforms.

HIGHER: European Heterogeneous Cloud/Edge Infrastructures for Next Generation Hybrid Services
Grant Agreement: 101189612, DG/Agency: HADEA
Start / end date: 01.01.2025 - 31.12.2027
Contact: Dr. Menelis Maszakis | maszakis@fORTH.gr
FORTH - Institute of Computer Science, GREECE

HIGHER (GA 101189612 / DG/Agency: HADEA): <https://higher-project.eu>

[RIA Project started on Jan. 1, 2025]

12th of June, 2026

RISC-V Summit Europe 2026 - Workshop

Closing remarks

- RISER has shown that a RISC-V-based Linux server for cloud services is achievable with European technology.
 - HIGHER takes this further by targeting OCP-compliant data center modules—both Arm-based using SiPEARL's Rhea and RISC-V-based using EUPILOT silicon.
-
- High-end chips are hard. Schedules slip. Supply chains are complex. We should not underestimate the difficulty of what remains.
-
- **IMHO** : *The question is whether we can sustain the commitment to see it through to production-ready, commercially viable systems.*



Thank you for your attention

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RISER: <https://riser-project.eu>

HIGHER: <https://higher-project.eu>